Synchronous Circuits Design Methodology, *Continued*

<u>Step 2- Divide the clock period among all logic levels including those in the FFs</u>:

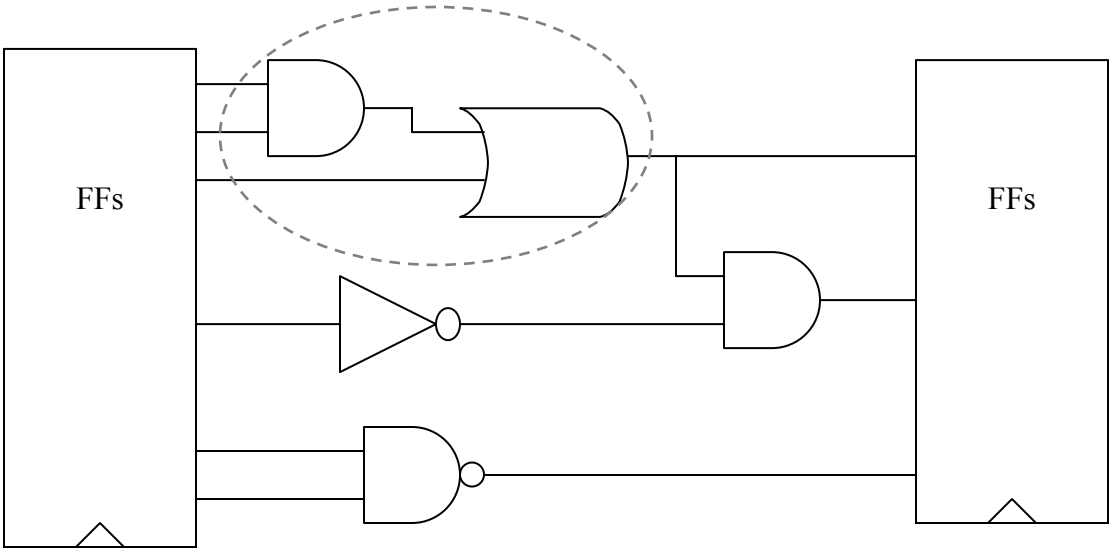
$TCK \geq T_{CK\rightarrow q1} + TD + T_{SU2} + Tskew + Tjitter\ p\text{-}p$

- Subtract Tskew and Tjitter first from TCK = T'CK
- Calculate the total number of logic levels in the **<u>WORST CASE</u>** logic paths **BETWEEN** any 2 FFs = number of logic levels in longest logic path + 2 logic levels (in Slave) for TCK➔q1 + 2 logic levels (Master) for TSU2
- Divide T'CK (clock period TCK – Tskew – Tjitter) by the number of the logic levels.

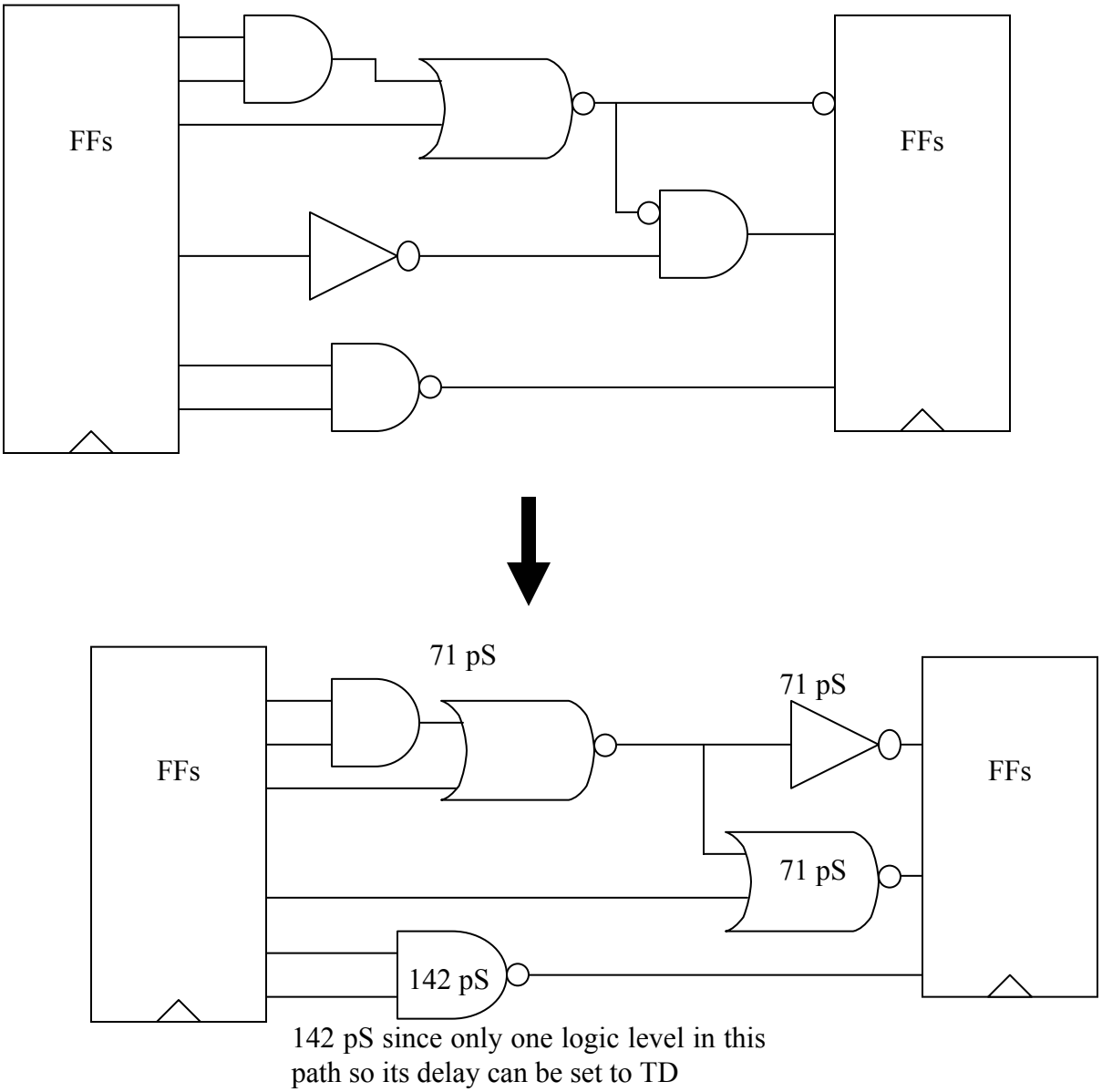
➔ This will give us the REQUIRED delay per logic level.

<u>Example 1:</u>

Convert the following to CMOS logic, and assign appropriate delays to each gate. Also find the required clock to Q and setup delays ($T_{CK\rightarrow q1}$, T_{SU}) The required clock frequency is 2GHz
Assume Tskew = 50 ps and Tjitter p-p = 20 ps



First perform logic transformation:



142 pS since only one logic level in this path so its delay can be set to TD

T'CK = TCK – Tskew – Tjitter
= 500 ps – 50 ps – 20 ps = 430 ps

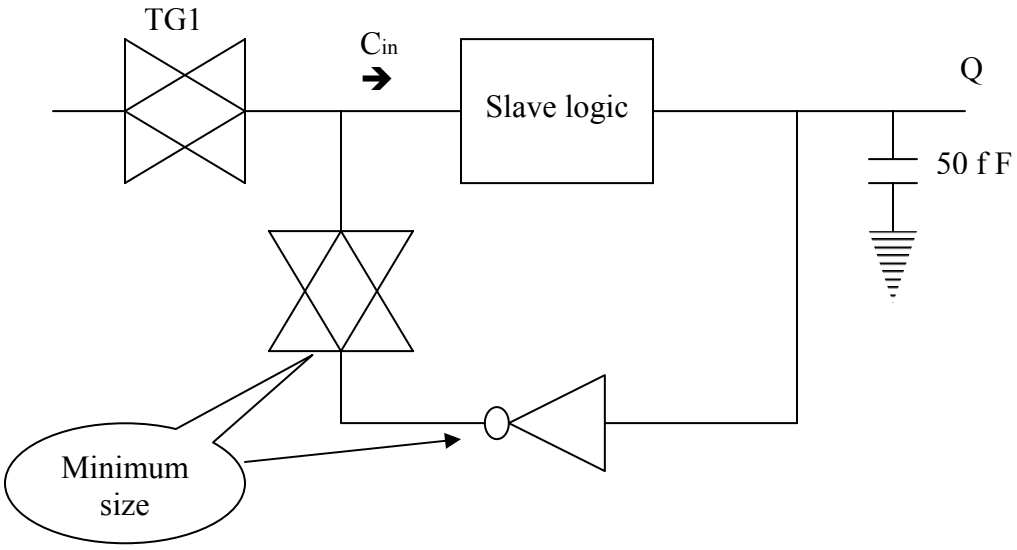
Total number of logic levels = 4 + 2 = 6

Delay per LEVEL = 430/6 ≈ 71 ps ➔ Tsu2 = 142 ps, $T_{CK \rightarrow q1}$ = 142 ps

If the FFs are already designed and the $T_{CK \rightarrow q1}$ and T_{SU2} are already known then
$T_D = T_{CK} - T_{CK \rightarrow q1} - T_{SU2}$ – Tskew – Tjitter
Then we divide T_D by the number of the logic levels in between the FFs to get the delay per logic level. We do not r-design the FFs

Step 3- Start Designing the FFs:

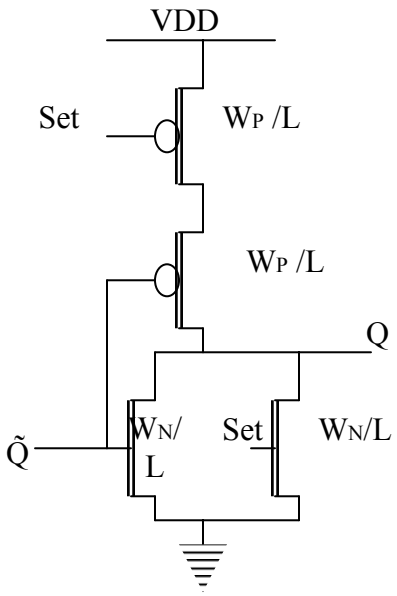
Assume a load capacitance (e.g. 50fF), then Design the salve logic with the assumed load



Once the slave logic is designed, we calculate its input capacitance
$C_{in} = C_{ox} * L (W_P + W_N)$

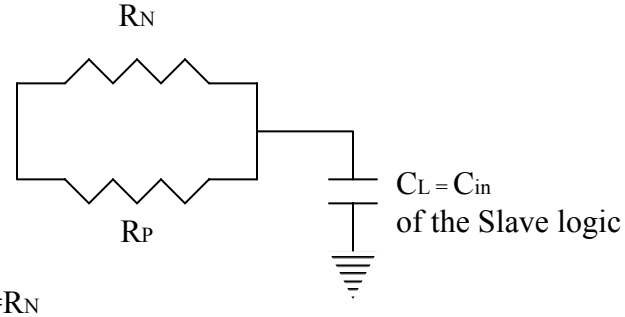
Example:

NOR Slave logic



This becomes the load capacitance for Master logic and T_{G1}

➔ Then Design T_{G1}:



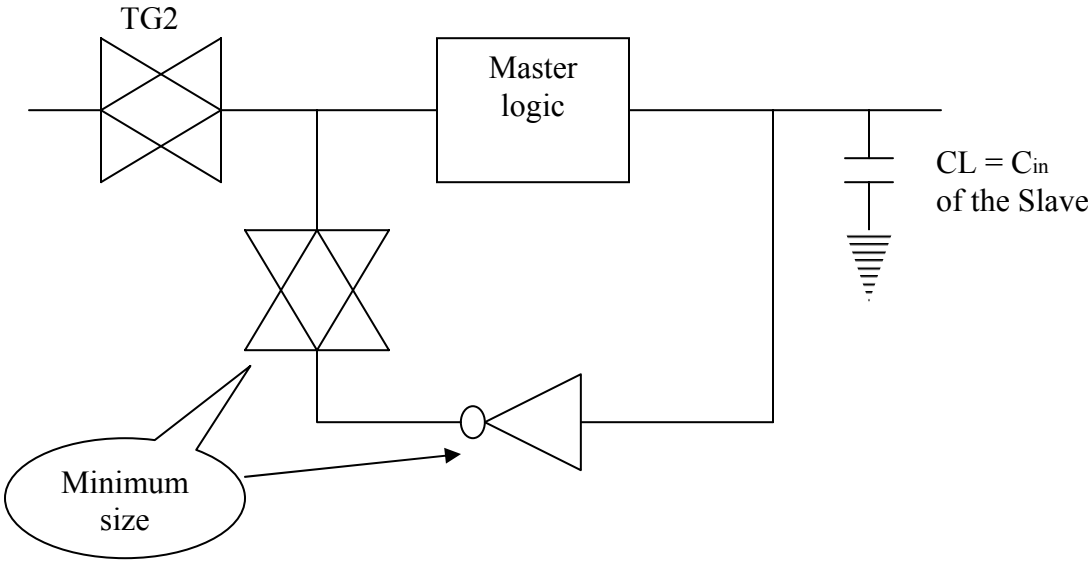
Let $W_P = 2\ W_N$ ➔ $R_P = R_N$

➔ $R_{total} = R_N/2$ ➔ $T_f = C_L * R_N/2$ ➔ $R_N = 2\ T_f / C_L$

➔ Then calculate as $W_N = \frac{VDD - V_{tn}}{2 I_{Dsat/um}\ * R_N}$ (NMOS)

➔ then calculate $W_P = 2\ W_N$

➔ Then Design the MASTER logic in the same way, followed by the design of TG2



➔Then Calculate Cin of the MASTER logic ➔this is Cin of the FF.