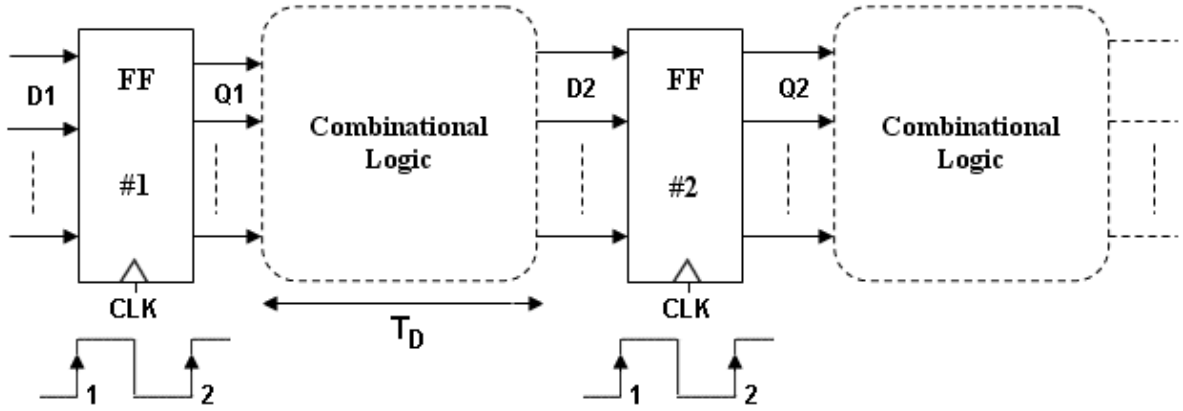
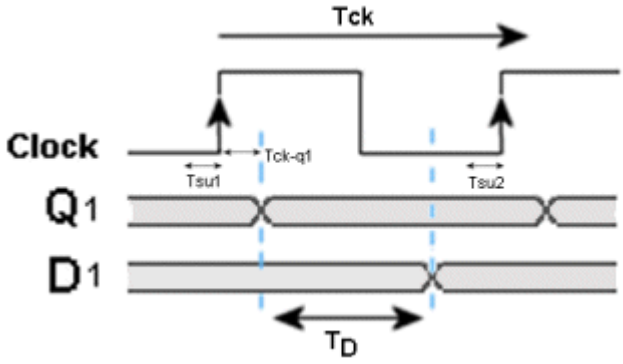
# Design of CMOS Synchronous Sequential Circuit:

- A synchronous sequential circuit basically looks like this:




- Based on the FF & combinational logic timing parameters, the following timing constraints are obtained for correct operation of the circuit:




$$\rightarrow T_{ck} \geq T_{ck \rightarrow q1} + T_D + T_{su}$$

$T_D$ = worst case delay through combinational logic

- This assumes that the clock arrives at all **FFs**, at exactly the same time!
- **Clock Skew** ($T_{skew}$) is the delay between clocks at different chip locations.
- To take Skew into account:

$$\rightarrow T_{ck} \geq T_{ck \rightarrow q1} + T_D + T_{su} + T_{skew}$$

- **Clock Signals** will have random variations in their **Periods** and **Frequencies**, called **Jitter**.
- We have to take into account the **Peak to Peak Jitter** ($T_{P\text{-}P\ Jitter}$):

$$\rightarrow T_{ck} \geq T_{ck \rightarrow q1} + T_D + T_{su} + T_{skew} + T_{P\text{-}P\ Jitter}$$

- Another **Timing Constraint** arises in situations where $T_D$ is "**Zero**" or very small when the output of a FF is fed directly to the input of another (e.g. in **Shift Registers**). In such situation, we need to make sure that the data does not pass

through two FFs (during the transparency window of the FF where both master and slave are enabled). Hence to avoid Hold Time violation:

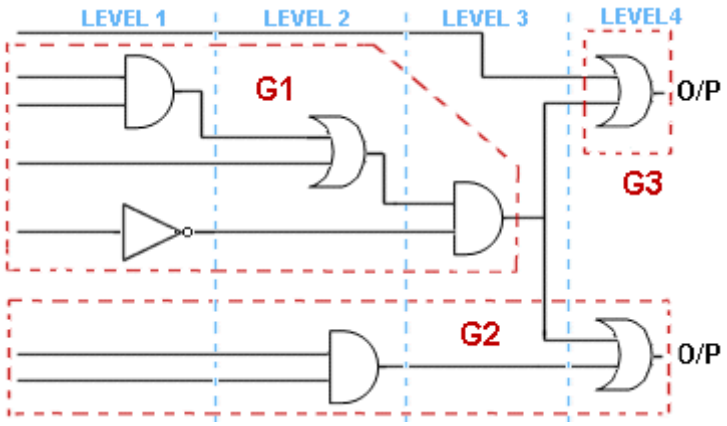
$$T_{skew} + T_{P\text{-}P\ Jitter} + T_{hold2} \leq T_{ck \rightarrow q1} + T_D$$

Where $T_{hold2}$ is the hold time of the 2nd FF

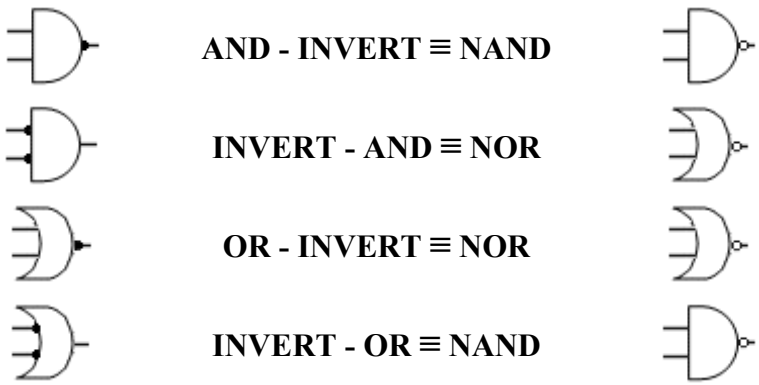
## ***Synchronous Circuit Design Mythology:***

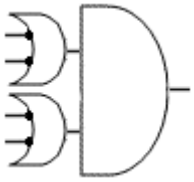
1) Through **Logic Transformations**, transfer the logic between the **FFs** into **CMOS Gates** with minimum number of **Logic Levels** And/OR minimum number of **Transistors**:

↳**1st.** Combine as many gates into single complete gates:
any cluster or group of gates that have single O/P can be combined into a single gate. Example:




↳**2nd.** Starting from Logic Level One (the closest to the I/Ps), convert into CMOS using the following logic transformations:

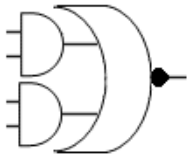




**INVERT - OR- AND**

**≡**

**AND - OR -INVERT**



**Similarly,**

**NVERT – AND - OR**

**≡**

**OR - AND - INVERT**

↳**3rd.** Gates are converted by inserting **<u>Bubbles</u>**, in pairs, either at the I/Ps or O/Ps & transfer the gates into **CMOS**.

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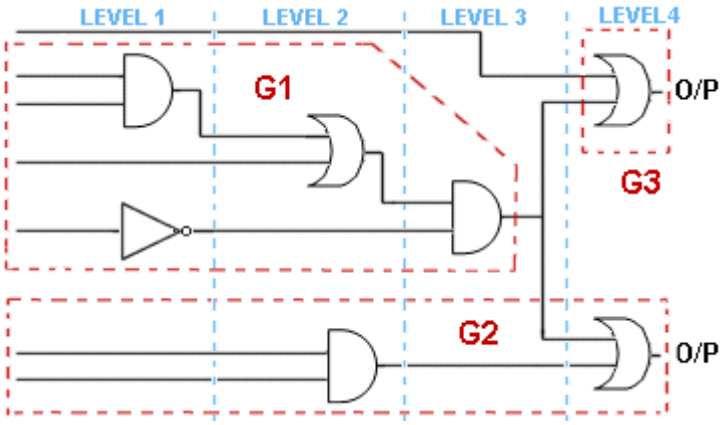
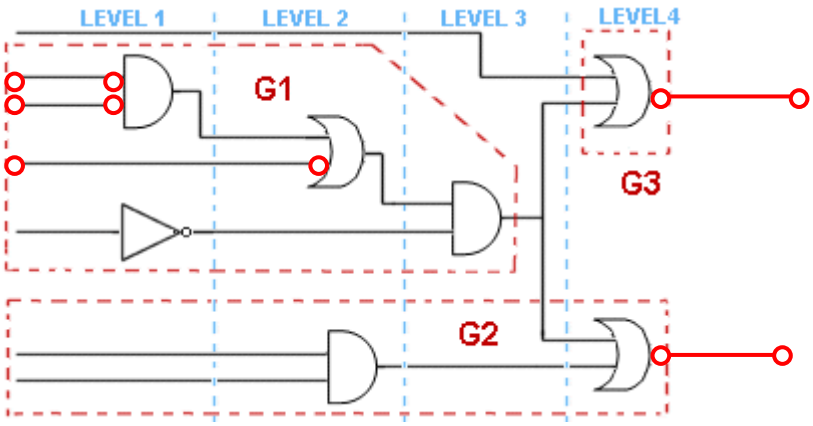
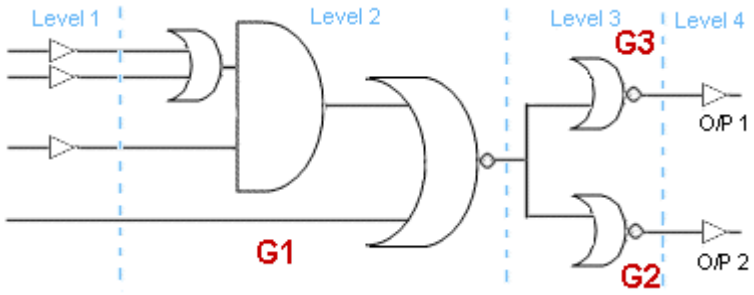
**Example1:**




- **G1:** **INVERT – AND – OR – AND ≡ OR – AND – OR – INVERT**
- **G2:** **AND – OR ≡ AND – OR – INVERT – INVERT**
- **G3:** **AND ≡ NAND – INVERT**



- **The Transformed Circuit:**




→ 4 Logic Levels → 28 Transistors ; Original Circuit had 4 Logic Levels

> ↳ The number of **Logic Levels** in the **Transformed Circuit** should not exceed the **Original Circuit** by, at most, more than **one extra level of inverters**.

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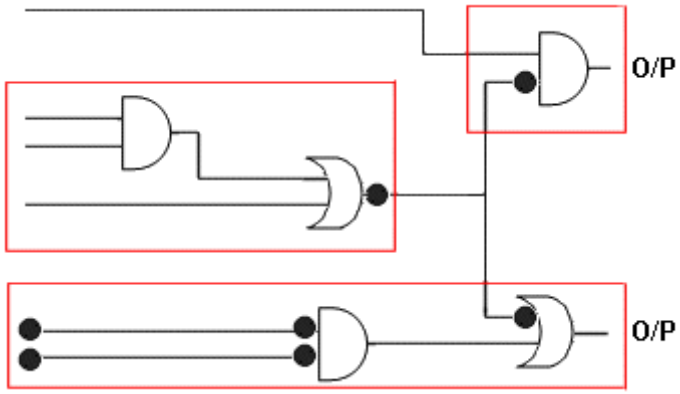
**Example2:** The following Circuit is implemented in CMOS (original circuit without the black bubbles):




- This is the Transformed Circuit: