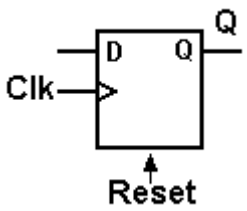
- **Example 2:** Implemented in CMOS; a **Positive Edge-Trigged FF** with **Active Low Direct Set & Reset** I/Ps. (with **Reset** priority)

Sol:



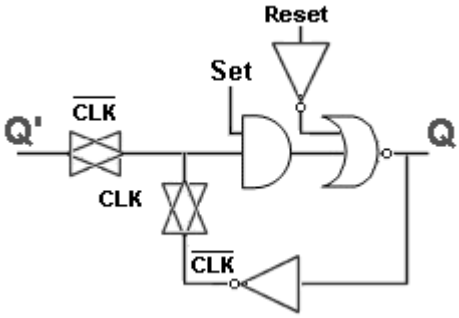
CLK	Set	Reset	Q
X	X	0	0
X	0	1	1
0	1	1	Q
↓	1	1	D

Reminder: for FF with Direct Inputs, whatever this I/Ps do for the slave → its complement should be done to the Master.

- **Slave Logic:**

Q'	Set	Reset	Q	
X	X	0	0	} Reset Active
X	0	1	1	} Set Active
0	1	1	1	} works as inverter
1	1	1	0	

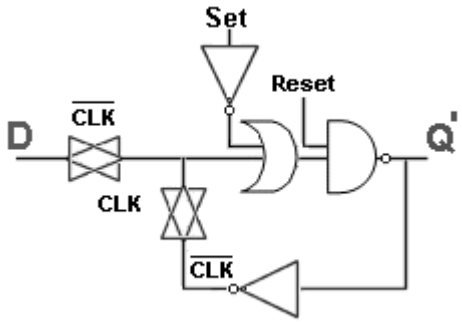
$$Q = Reset.\ \overline{Set} + \overline{Q'}\ .\ Set.\ Reset$$
$$= Reset\ (\overline{Set} + \overline{Q'}.\ Set)$$
$$= Reset\ (\overline{Set} + \overline{Q'})$$
$$= \overline{\overline{Reset} + Set\ \cdot\ Q'}$$



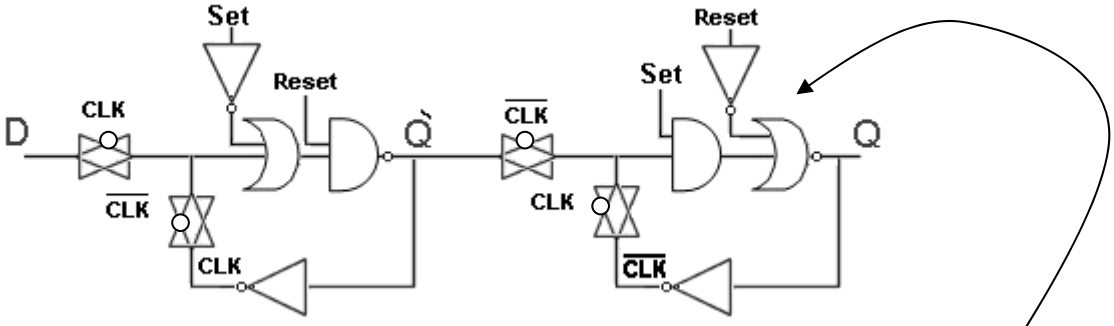
- **Master Logic:**

D	Set	Reset	Q'	
X	X	0	1	} Reset Active
X	0	1	0	} Set Active
0	1	1	1	} works as inverter
1	1	1	0	

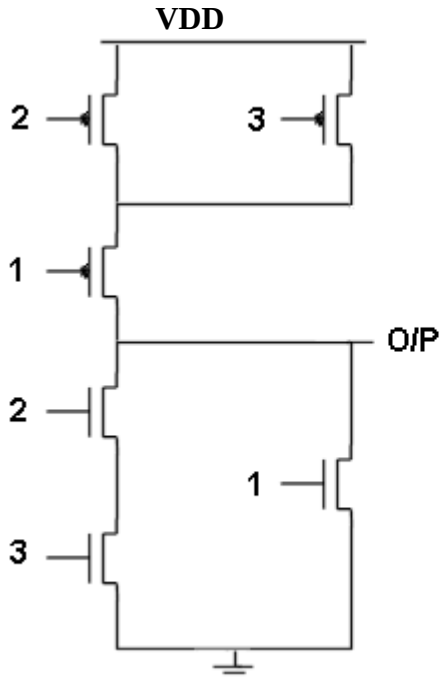
$$Q' = \overline{Reset} + \overline{D}.\,Set.\,Reset$$
$$= \overline{Reset} + \overline{D}.\,Set$$
$$= \overline{Reset\,.\,(D + \overline{Set})}$$

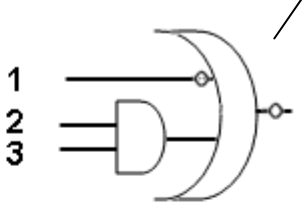


- **The final solution:**

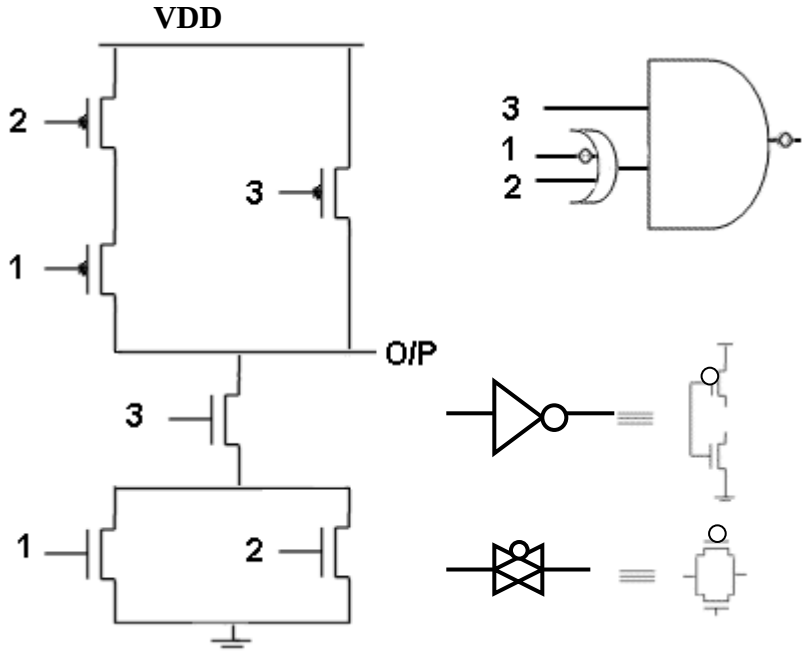


- **The AOI 21**





- **The OAI 21**



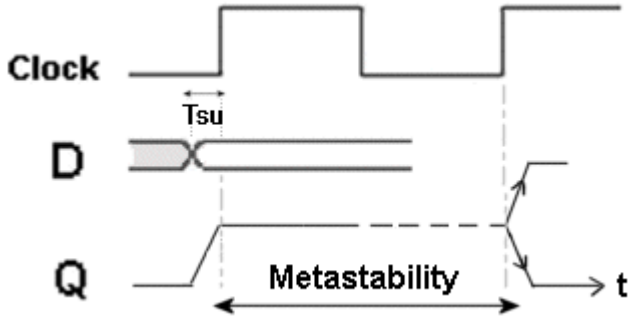
FF Timing Parameters:

- when using **FF** in synchronous sequential circuit, there are **Three Timing Parameters** that we need to deal with:

1) Setup Time (Tsu):

The minimum time before the active clock edge**;** where the data has to stabilize → related to the delay through the **Master** logic**.**

- **Tsu** violation could result in Metastability → **Q** not being 0 or 1



2) Hold Time (T_{hold}):

The minimum time the data needs to be held constant after the active clock edge → related to the delay between **CLK & CLK'** when both **Master & Slave** are enabled.

- T_{hold} violation may cause the new data to propagate to **Q** (2 changes in Q during one clock cycle) or **Metastability** to occur.

3) Clock to Q delay ($T_{ck \rightarrow Q}$):

This is the time it will take Q to change after the arrival of the active clock edge → this time is related to the propagation delay of the **Slav**e logic