Standard Naming of Logic Functions:

A combination of letters and numbers are used to describe the function and the number of I/Ps.

Letters: A = AND , O = OR , I = Invert

Ex1. AOI 222 : 3 AND terms, that are ORed then Inverted

We have 3 logic terms each has 2 I/Ps.

$$F = \overline{(1.2) + (3.4) + (5.6)}$$

A A A

OR

Ex2. OAI 123 → 3 OR terms that are Anded then Inverted

$$F = \overline{1.(2+3).(4+5+6)}$$

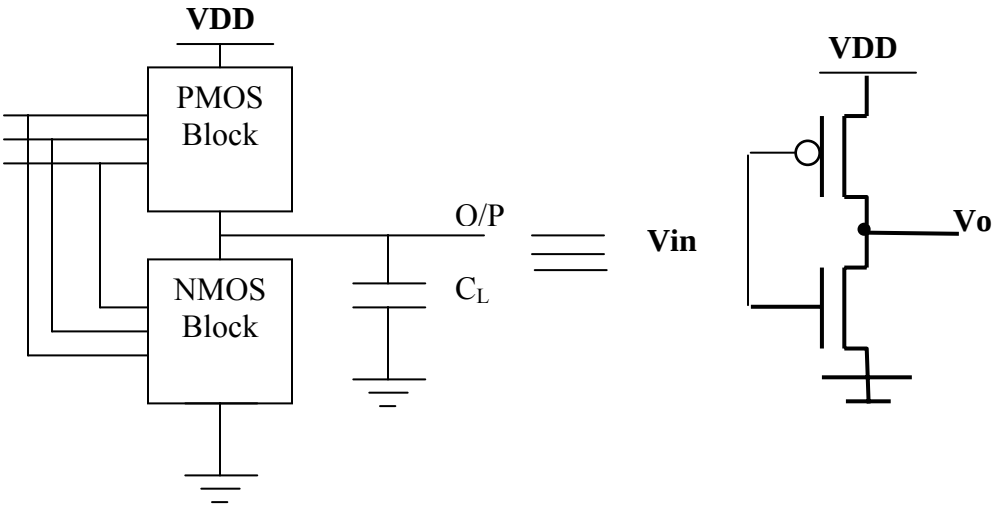
Ex3. AO 223

$$F = \overline{(1.2) + (3.4) + (5.6.7)}$$

CMOS Logic Circuit Design:

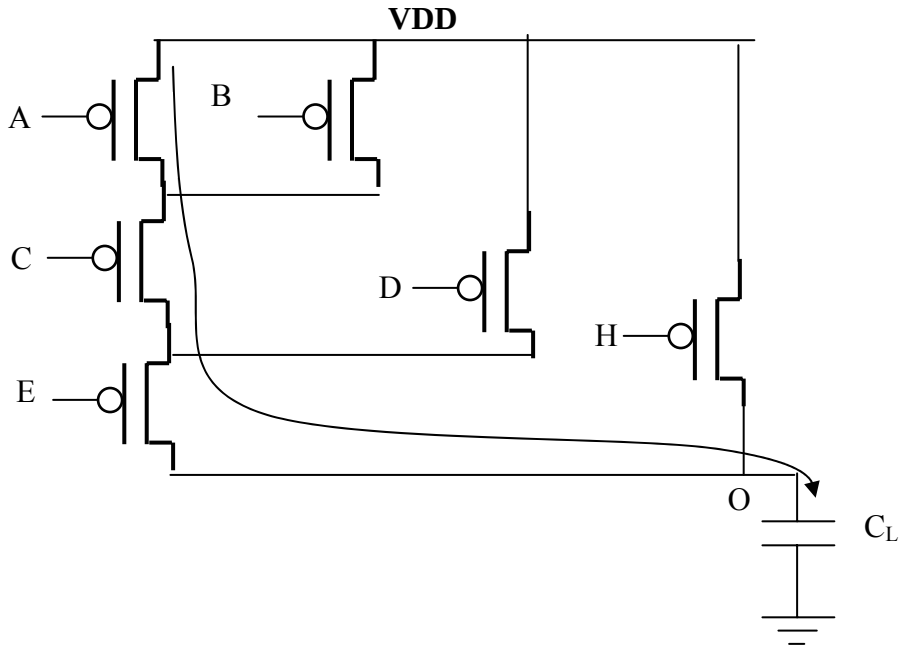
Delay Calculation for CMOS Gate:

In order to calculate the delay of the CMOS gate, we find an equivalent inverter (with equivalent pull-up and pull-down resistances) and calculate $T_D=0.5\ C_L(R_P+R_N)$

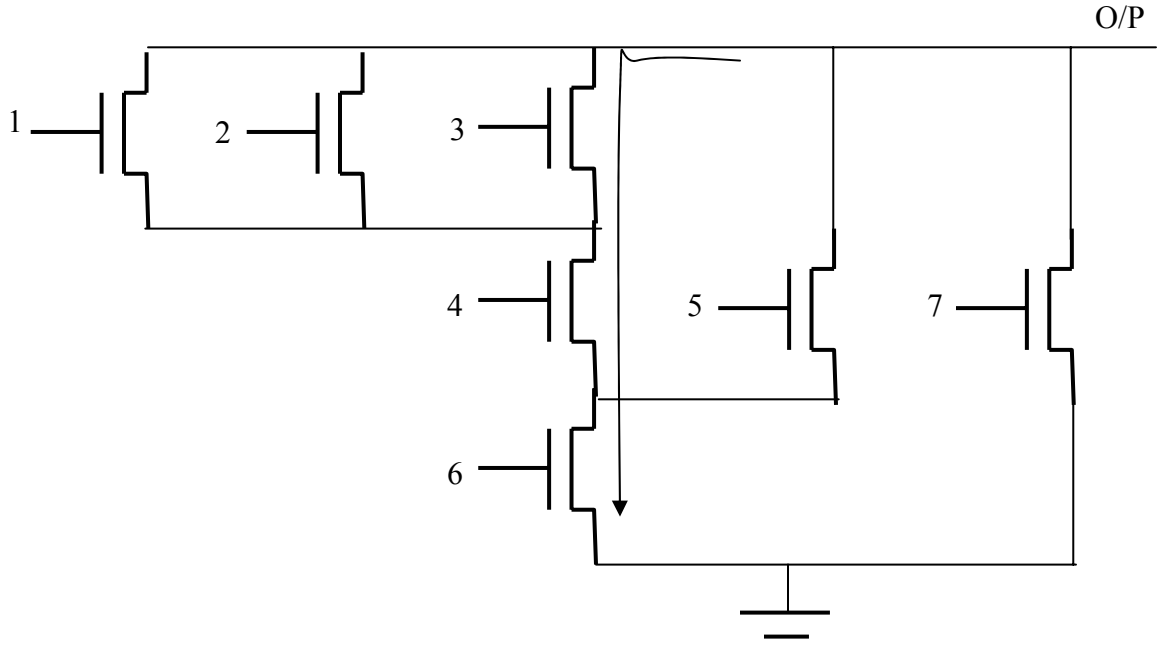


Where T_r and T_f of the equivalent inverter = worst case Tr and Tf of the gate.

- Worst case T_r occur when the O/P is charged (or pulled-up) through the longest chain of series PMOS transistors: e.g. for the PU block below, worst case charging is when B = D = H = 1 And A = C = E = 0 i.e. charing through A,C, & E.



- Similarly, worst case T_f occurs when discharging the output through the longest discharging path. For the PD block below, Worst case : 1,4,6 are ON or 2,4,6 or 3,4,6 while every other transistor is off



$$R_{P_{eff}} = \frac{V_{DD} - Vth}{2\, I_{SD_{Sat/Um}}{}_{pmos} * Wp_{eff}}, \qquad R_{N_{eff}} = \frac{V_{DD} - Vth}{2\, I_{DSat/Um}{}_{nmos} * W_{N_{eff}}}$$

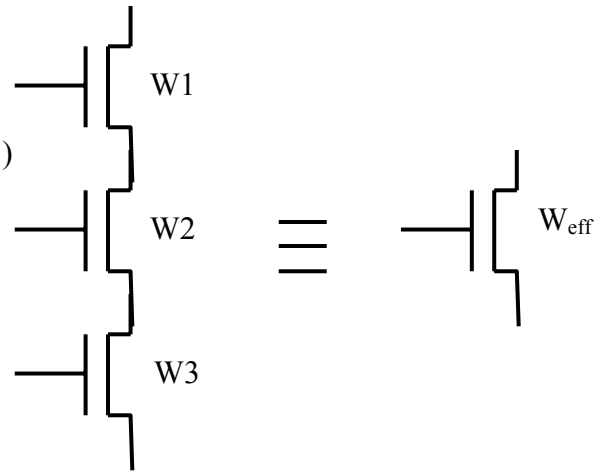
W_{eff} of any series connected transistors is obtained as follows:

$R_{eq1} + R_{eq2} + R_{eq3} = R_{eff} \rightarrow$

$(V_{DD} - V_{th} / 2.I_{Dsat}).(1/W_1 + 1/W_2 + 1/W_3) = (V_{DD} - V_{th} / 2.I_{Dsat}.\ W_{eff})$

$\rightarrow\ 1/W_{eff} = 1/W_1 + 1/W_2 + 1/W_3 \ldots..$

If $W_1 = W_2 = W_3 = W_N \rightarrow\ W_{eff} = W_N/3$



Ex1. Calculate the maximum frequency of operation of an AOI 222 CMOS gate with a 100 fF load, assuming that all NMOS transistor are 9 μm wide and 1 μm long. All PMOS transistors are 10/1 μm use the 1 μm technology.

$I_{SD_{sat}} = 200\ \mu A/\mu m$, $V_{tN} = |V_{tP}| = 0.8V$, $V_{DD} = 5V$

$T_{D\,avg} = 0.5\, C_L (R_P + R_N)$

$R_{P\,eff} = V_{DD} - |V_{tP}| / (2.I_{SD_{sat}} . W_{P\,eff})$,from the circuit schematic below:

$W_{P\,eff} = W_P / 3 = 10/3 = 3.33\ \mu m$

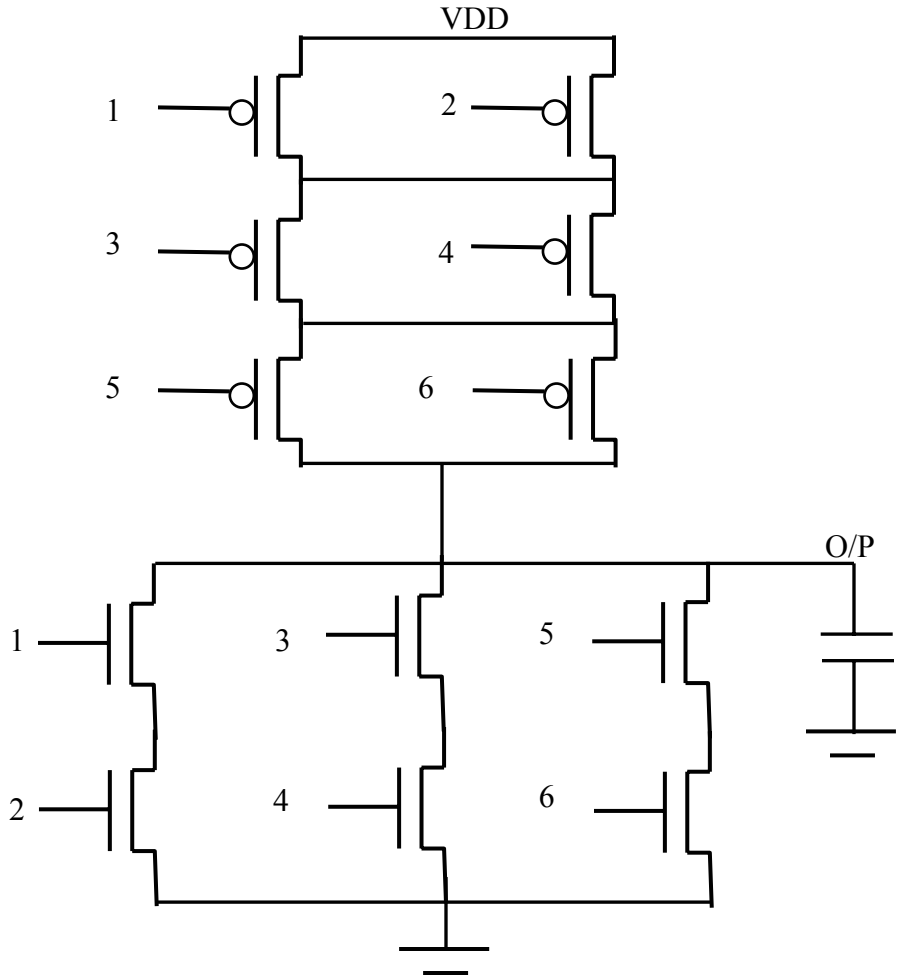
$R_{P\,eff} = 4.2 / (400x10^{-6} \times 3.33) = 34\ K\Omega$

$R_{N\,eff} = (V_{DD} - V_{tN}) / (2.I_{DS_{sat}} . W_{N\,eff})$, $W_{N\,eff} = W_N/2 = 2.5\ \mu m$

$R_{N\,eff} = 4.2 / (100x10^{-6} \times 2.5) = 1.6\ K\Omega$

$F_{max} = 1/T_{D\,avg} = 1 / (T_r + T_f) = 1 / C_L (R_{P\,eff} + R_{N\,eff})$

$F_{I/P\,max} = 1 / (100x10^{-15} .(3.4+1.6)x10^3)$


VDD
1
2
3
4
5
6
O/P
1
3
5
2
4
6