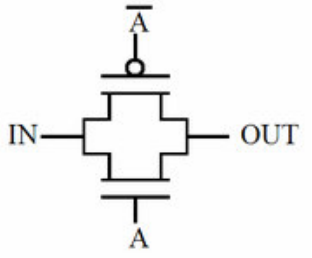
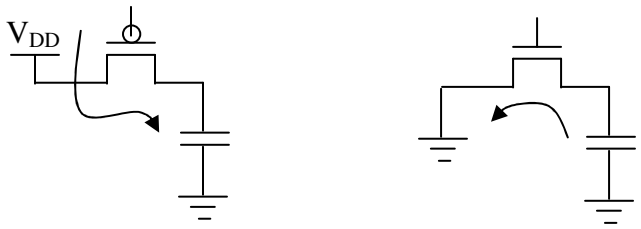
CMOS Transmission Gates:

- A Transmission Gate (TG) is a complementary CMOS switch.

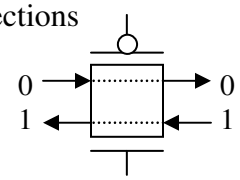


PMOS and NMOS are in parallel and are controlled by complementary signals

- Both transistors are ON or OFF simultaneously.
- The NMOS switch passes a good zero but a poor 1.
- The PMOS switch passes a good one but a poor 0.



- Combining them we get a good 0 and a good 1 passed in both directions
-
-



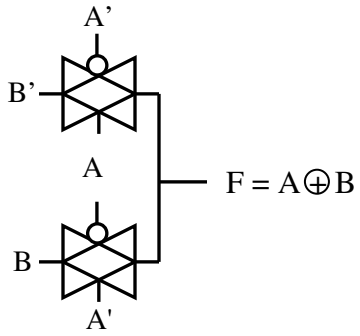
- Circuit Symbols for TGs:

- TGs are efficient in implementing some functions such as multiplexers, XORs, XNORs, latches, and Flip-Flops.

- **2 I./P XOR using TGs:**

  F = A.B' + A'.B , we need this: if A=1 → F = B' (pass B' to F)
  if A=0 → F = B (pass B to F)

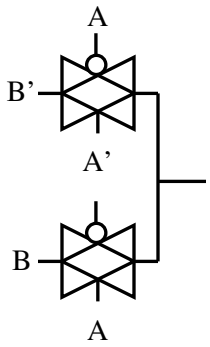
  using TGs:



8 Ts (2 inverters for A and B and two TGs)
Versus 12 Ts for regular CMOS

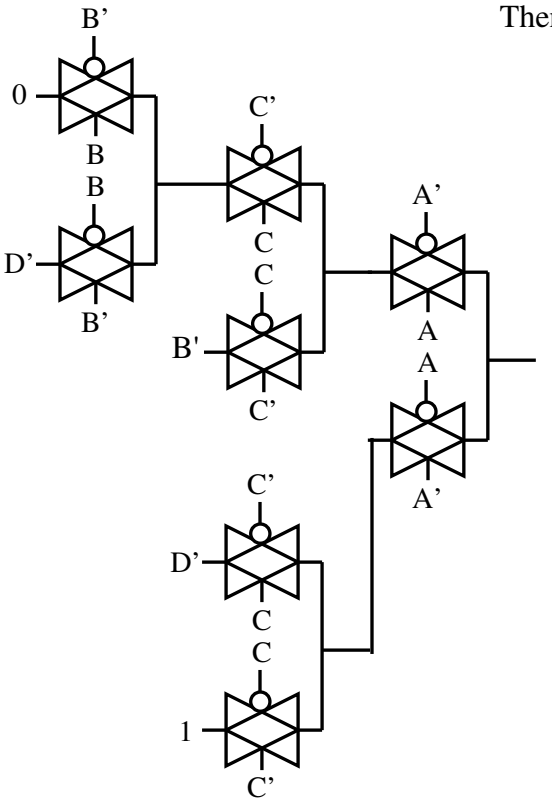
- **2 I/P XNOR**

F = A.B + A'B' if A=1 → pass B to F
if A=0 → pass B' to F



- **General Logic using TGs: AOI 22:**

F = (AB + CD)' if A=1 F = (B+CD)'
Then if C=1 → F= (B+D)' … and so on….

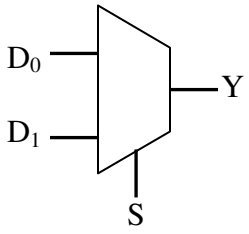


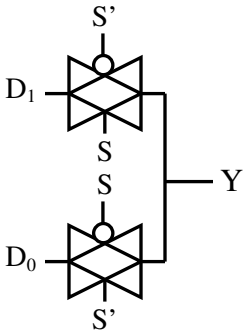
24 Ts versus 8 T for regular CMOS → TGs are very inefficient for regular functions

- **2-1 mux using TGs**

F = S'.D_0 + S.D_1

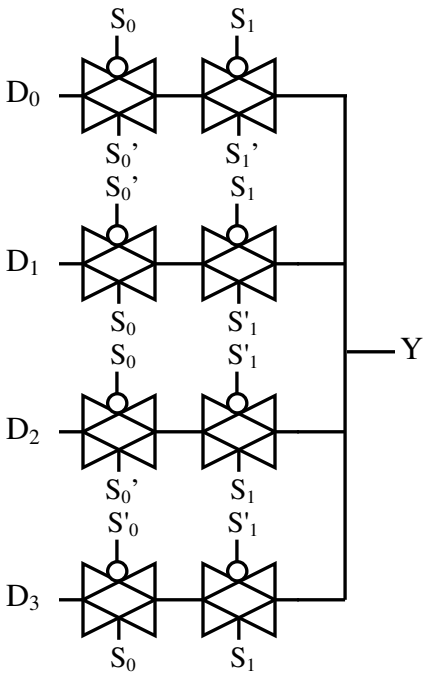
S	Y
0	D_0
1	D_1

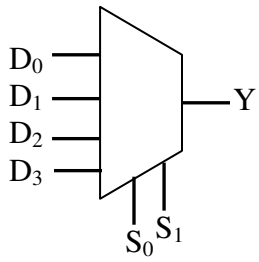




- **4-1 Mux in TGs:**

$$Y = S_1'.S_0'.D_0 + S_1'.S_0.D_1 + S_1.S_0'.D_2 + S_1.S_0.D3$$

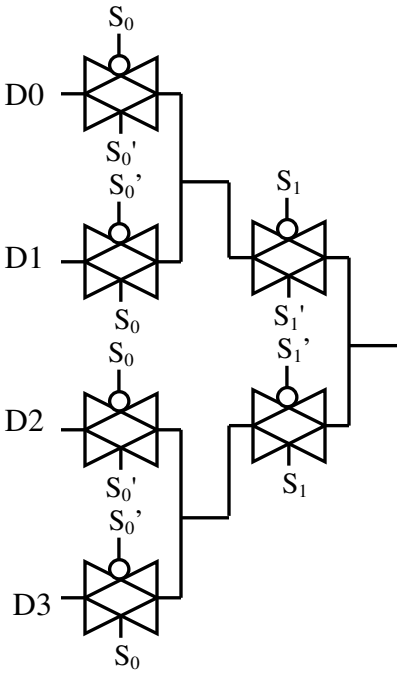


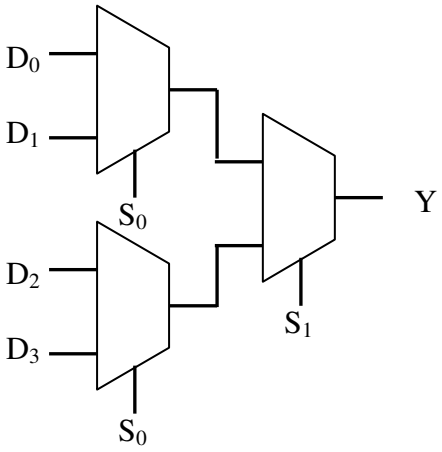


S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

20 Ts

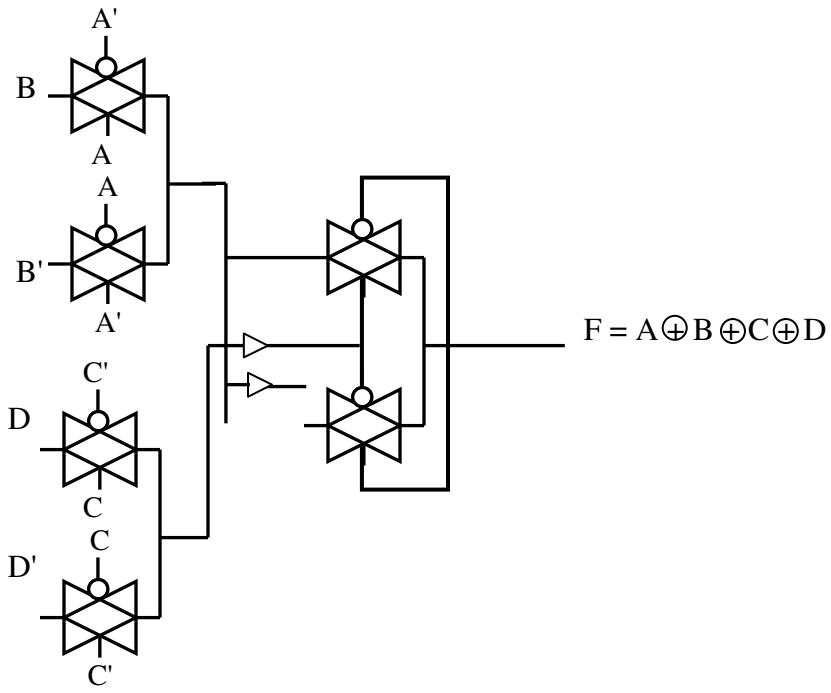
- **Another way is to use 3 of 2-1 Muxs:**





We can use the same concept to make 3,4 or more I/Ps XORs

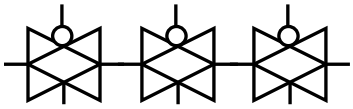
- **4 I/P XOR:**



F = A.B’.C’.D’ + A’.B.C’.D’ + A’.B’.C.D’ + A.B.C.D’ + A.B.C.D’ + A.B.C’.D + A.B’.C.D

In regular CMOS: 4 inverters + 64T = 72 T

Warning: TGs can not be connected in series for more than 3 levels →



If you need more than that, use CMOS inverters in between as buffers: