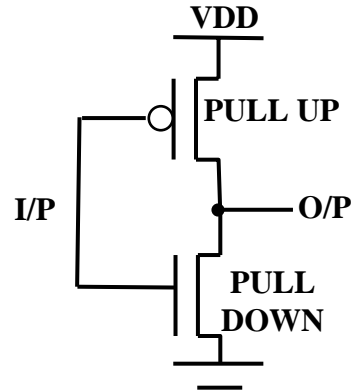
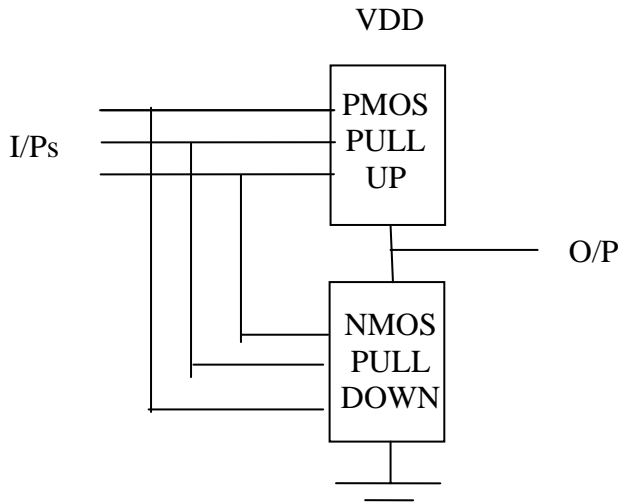


# Complex CMOS Logic Gate

## Basic Structure



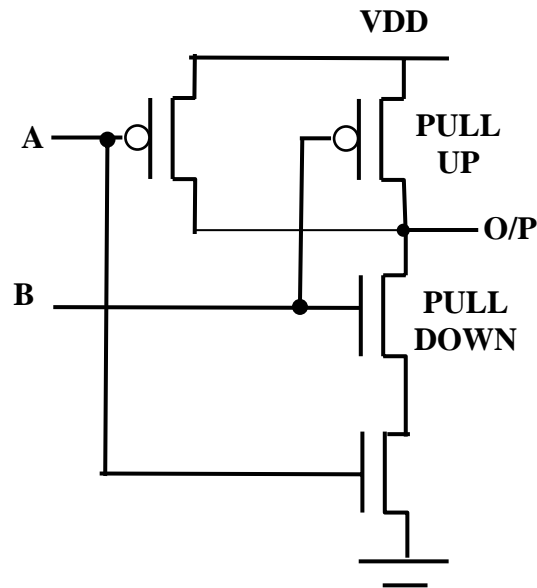
The Pull-Up (PU) block is a network of PMOS transistors

The Pull-Down (PD) block is a network of NMOS transistors

## Simple Gates

1) 2 I/P NAND  $F = \overline{A B}$

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



$F = 0$  only if both A & B = 1

→ 2 NMOS transistors in series

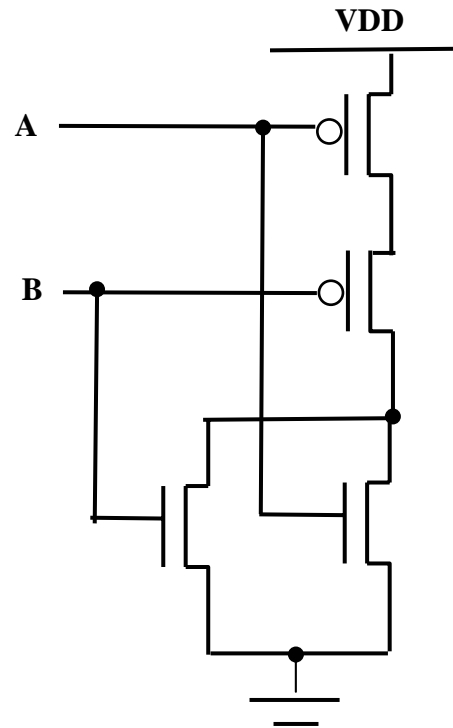
The PMOS block is always the complement of the N-MOS block

→ 2 PMOS transistors in parallel.

2) 2 I/P NOR  $F = \overline{A + B}$

| A | B | F |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

F = 1 only if both A & B = 0



2 PMOS in series & the NMOS block is the complemented ( i.e parallel )

**Methodology for obtaining the CMOS implantation of any Boolean expression:**

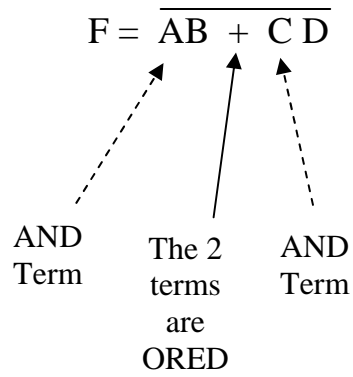
1) Any Boolean expression that is complemented ( i.e in the form  $\overline{(A+B).C}$  ) can be implemented using a single CMOS Gate (i.e a circuit with only one output F) → If the function is not complemented and/or some of the I/P's are complemented (e.g  $(A+B).C$  or  $\overline{(\overline{A+B}).C}$  )

Then It cannot be implemented using a single CMOS Gate → we have to do some logic transformation to implement it using minimum number of Gates or logic levels.

2 ) The output of a CMOS Gate is always complemented i.e we get the complement automatically

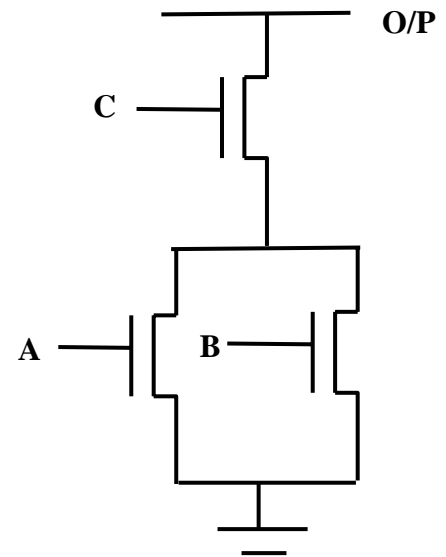
3) implement the NMOS block :  
 AND terms → series connected NMOSFET's  
 OR terms → paralleled connected PMOSFET's

Terms that are ANDed are connected in series  
 Terms that are ORed are connected in parallel



example

$$\overline{(A + B) \cdot C}$$

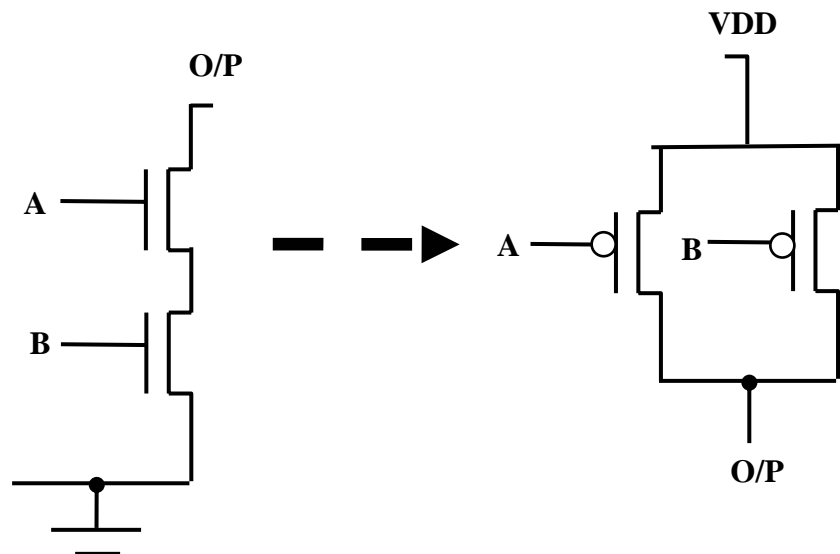


4) The PMOS block is the complemented of the NMOS block

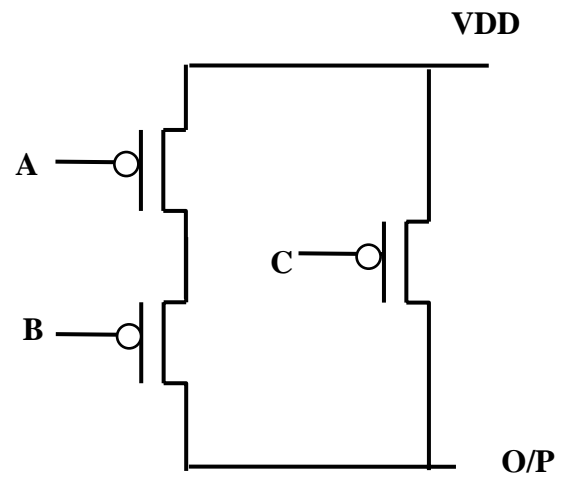
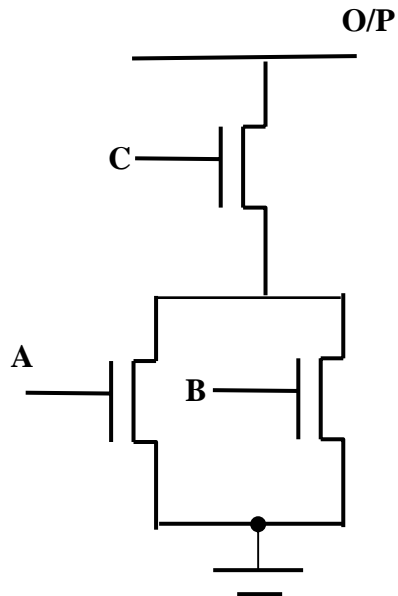
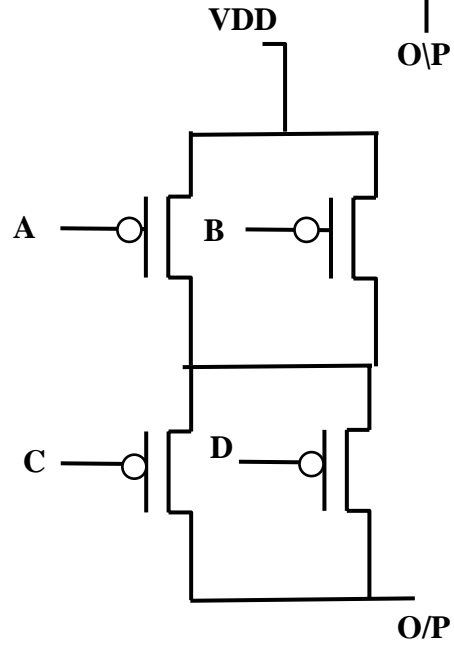
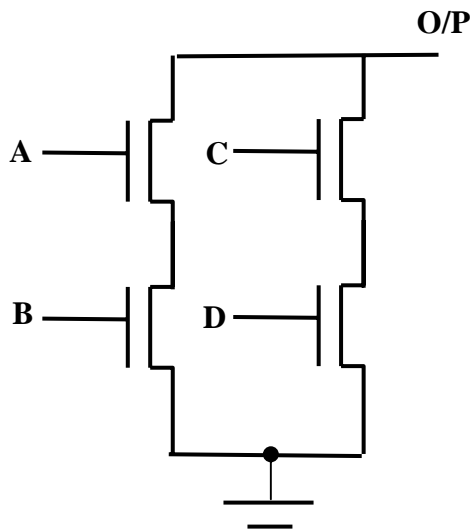
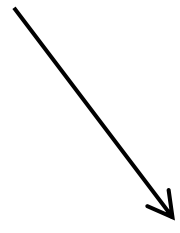
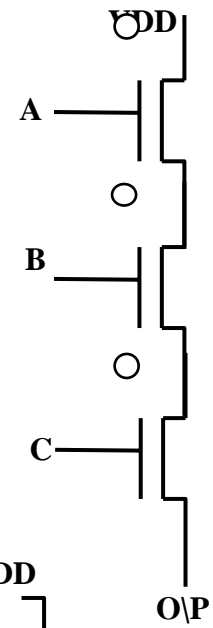
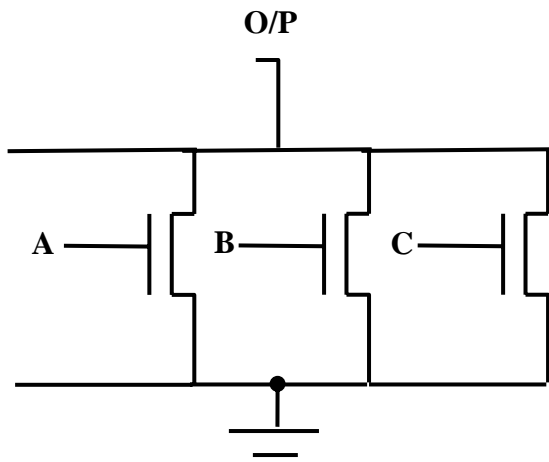
Series terms  $\rightarrow$  become Parallel  
 Paralleled terms  $\rightarrow$  become Series

Terms that are connected in series  $\rightarrow$  become connected in parallel  
 Terms that are connected in parallel  $\rightarrow$  become connected in series

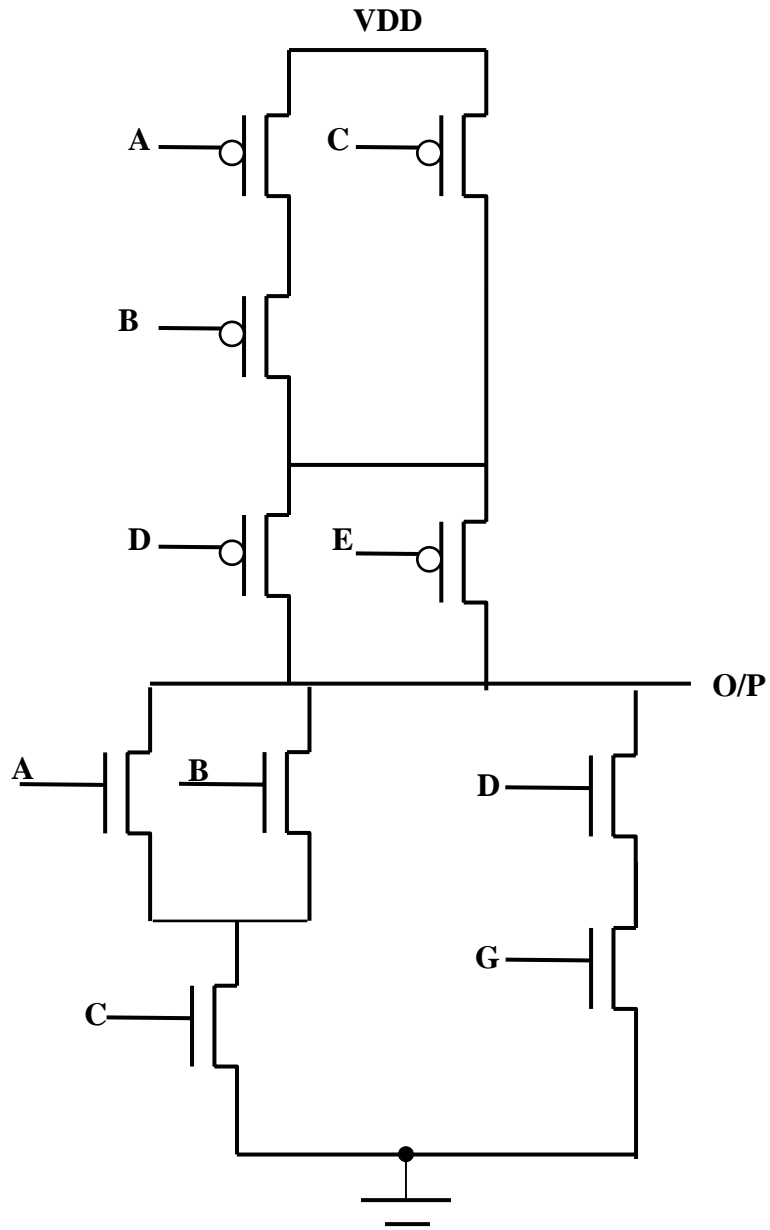
Examples



Order is not important in functionality,  
it is only important in performance.



Ex1] Implement:  $F = \overline{(A + B) \cdot C} + D G$



Ex2]

$$F = A ( B + C ( D + G.E ) )$$

