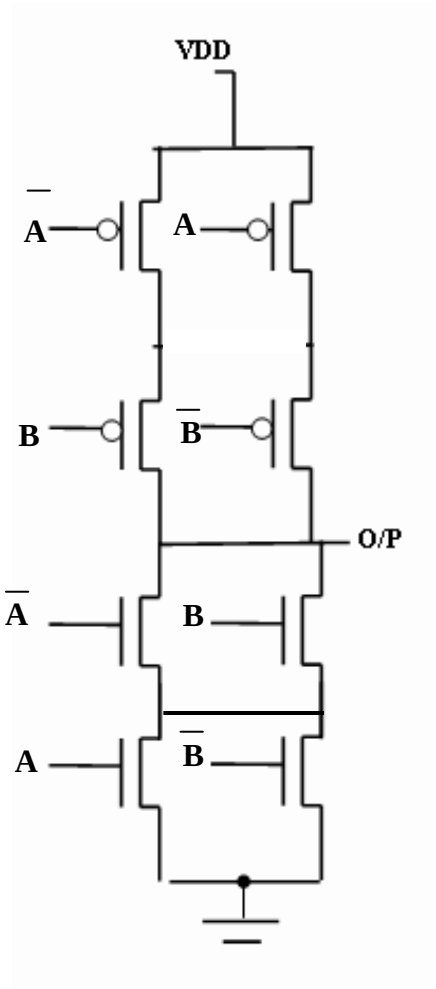
Ex4: Implement a 2 I\P XOR in CMOS

Sol: $F + A\overline{B} + \overline{A}B$

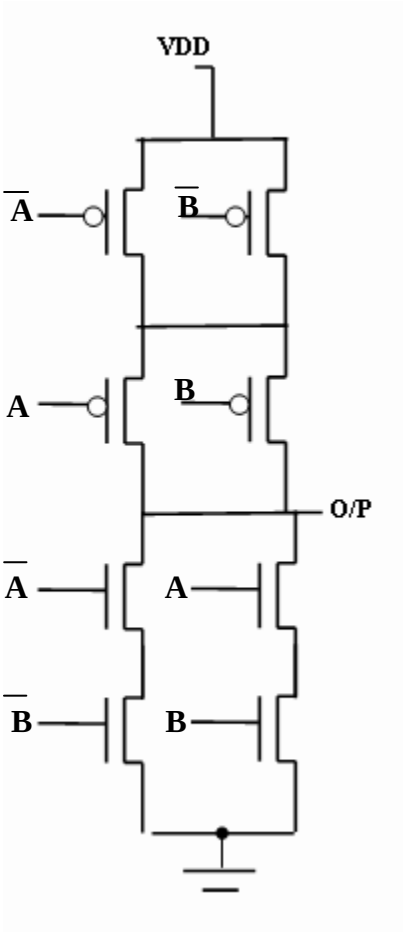
F is not complemented and some of the I\P's are complemented.
we need to do some logic transformations:

$F = [\ A\overline{B} + \overline{A}B\ ]$ (expand the 1st complement) → $F = \overline{(\overline{A}+B)(A+\overline{B})}$



# of transistors = 12 T
# of logic levels = 2
# of gates = 3 (including two inverters for the inputs)

Another XOR implementation (basically as the complement of the XNOR i.e. $\overline{\overline{A}\,\overline{B}+A\,B}$)



Ex5) Implement F = $\overline{A}$ (B + C + D) + $\overline{E}$ Using minimum # of transistors.

Sol : F is not complemented and some I\P are complemented .
2 choices for logic transformation

$$F = \overline{\overline{A}\,(B + C + D) + \overline{E}}$$

F has five literals (the occurrence of each variable in the Boolean expression is a literal weather the variable is in true or complemented form). E.g. the 2 I/P XOR had 4 literals.

1) implement $\overline{F}$ then invert

→ the # of T = 4 T (to invert A & E)
+ 10T (to implement the expression with “5literals”)
+ 2T to invert the O/P = 16T

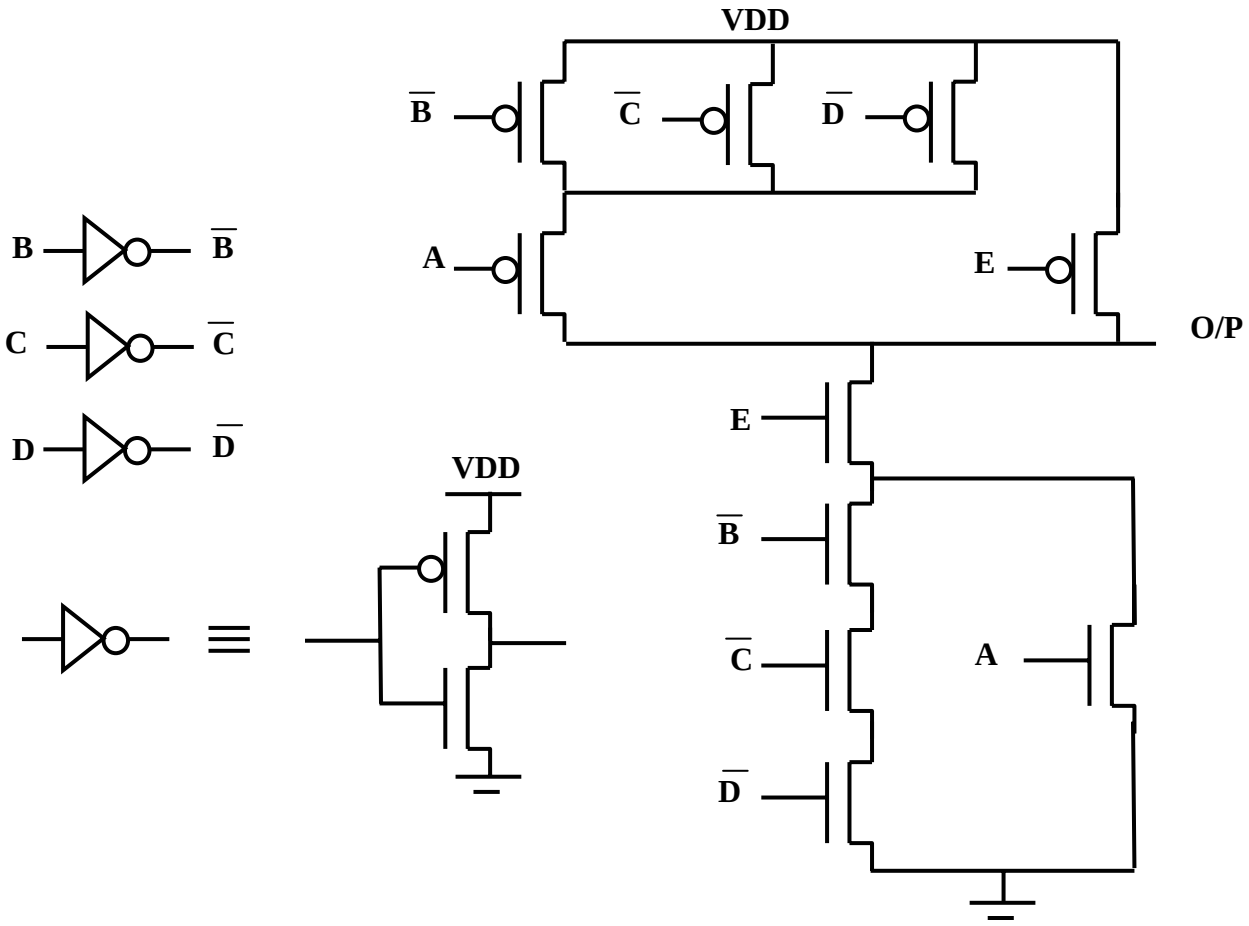
3 logic levels , 4 Gates

2) Expand the 1st complement then implement $F = [\, A + \overline{C}\ \overline{B}\ \overline{D}\ ]\ .\ E$

# of T = 6 T for I\P : C , B & D inversions
+ 10T for expression = 16 T

# of gates = 4 gates
# of logic levels= 2

choose 2) since it has lower # of logic levels



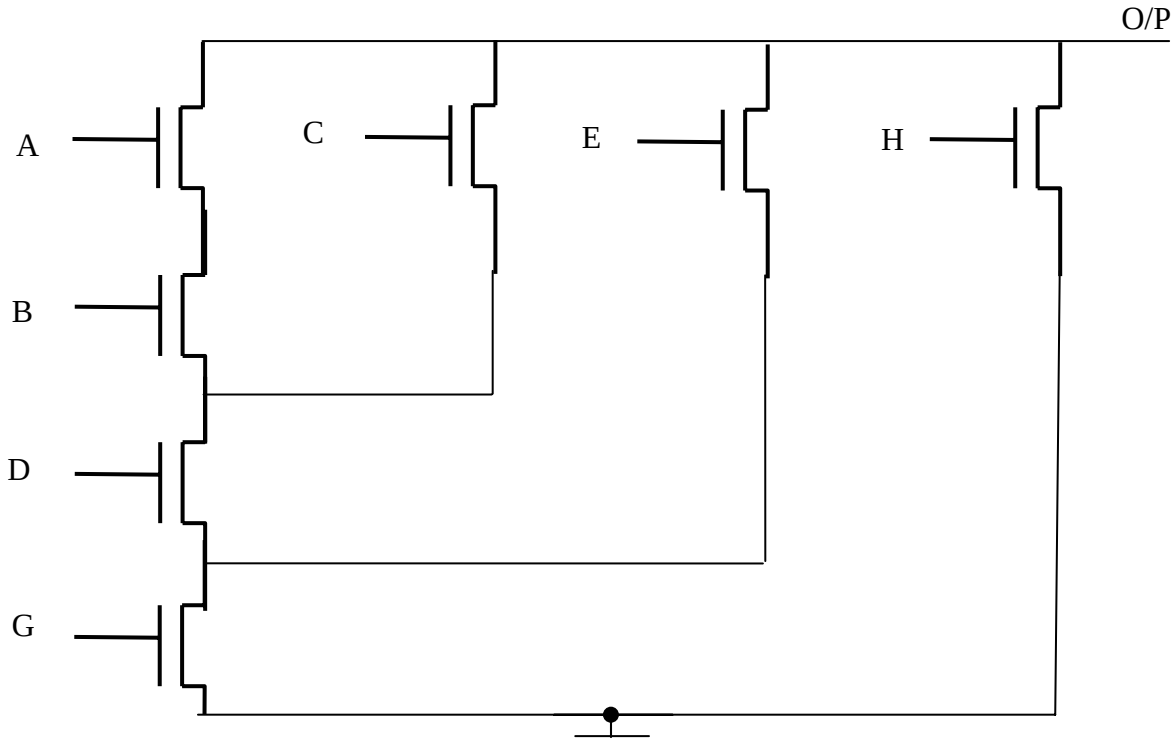
Ex6) Redo Ex5 assuming that inputs are available in true and complement form

Sol: first choice # of transistors = 10 T for expression
+ 2 T for O\P inverters

→ 12 transistors → 2 gates → 2 logic levels

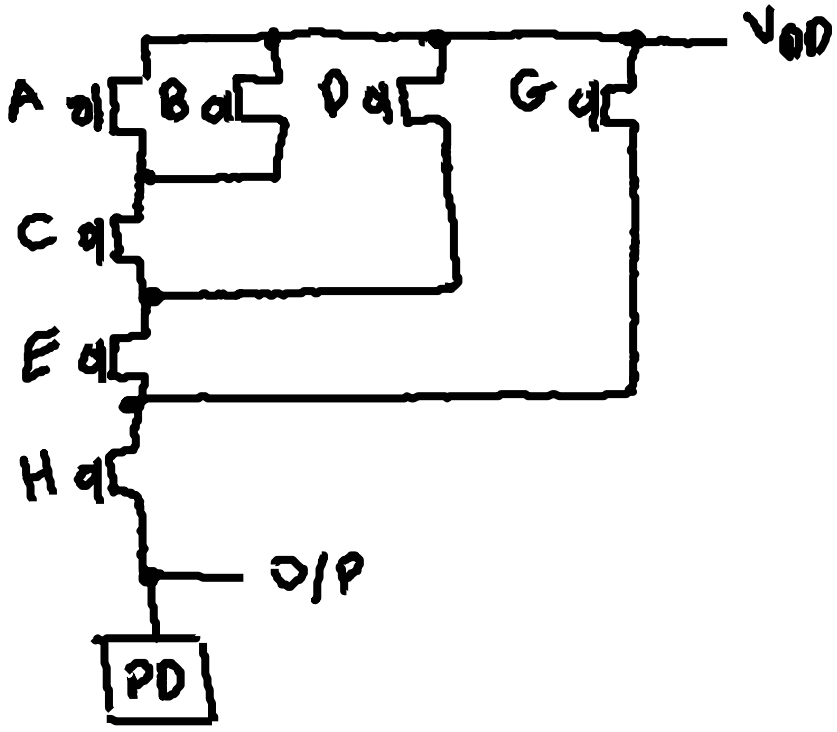
Second choice # of transistors = 10 T and 1 logic level (1 gate)
So we choose 2nd choice with no need for input inverters..

Ex7) in the following PD block of a CMOS Gate, find the function of this circuit & obtain the pull up (PU) block



$$F = \overline{[\,(AB + C)\,D + E\,]\,G + H}$$

PU:



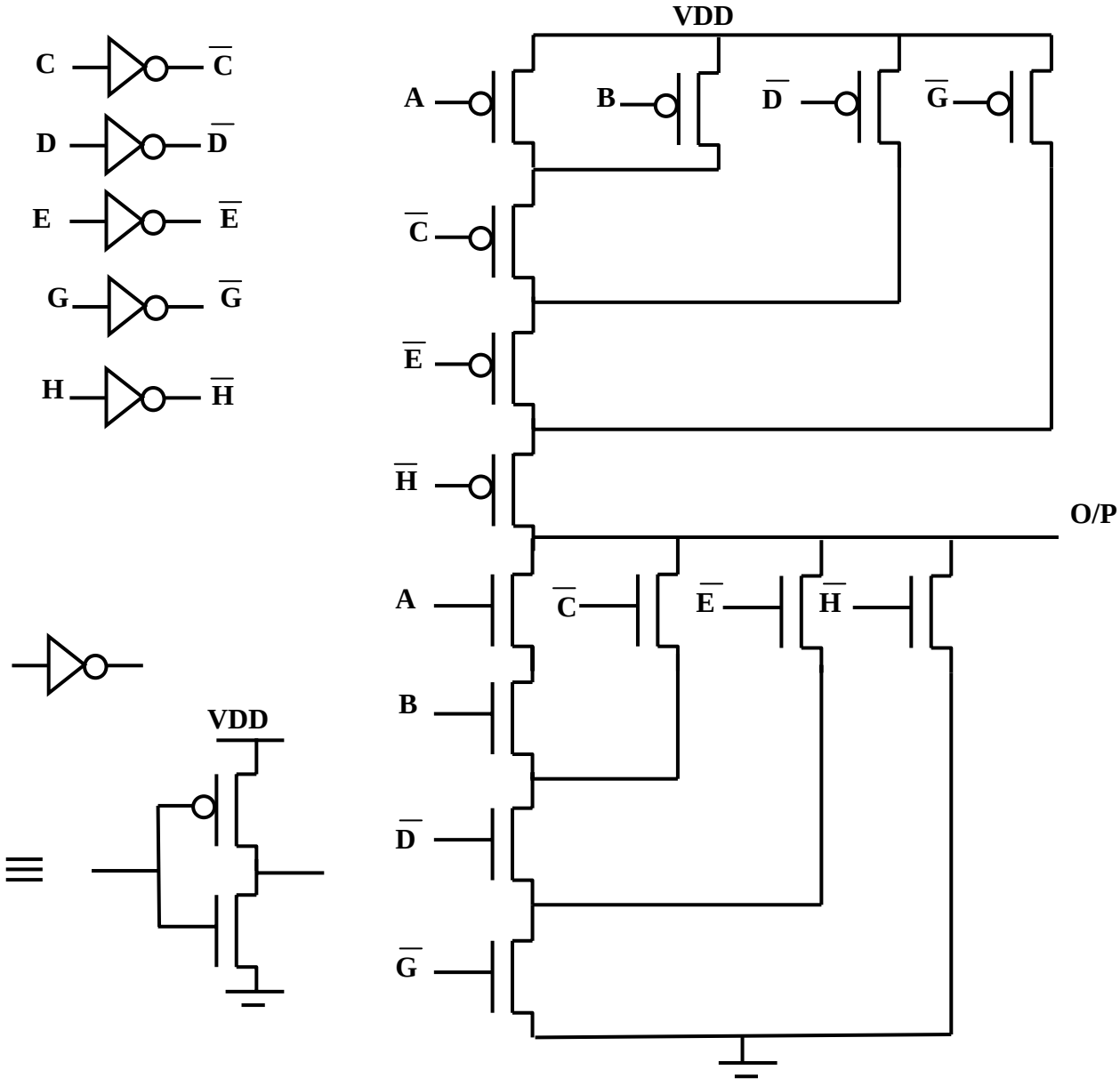
Ex8) implement the following function in CMOS using minimum number of logic levels

$$F = \{ [(\overline{A} + \overline{B}) C + D] . E + G \} H$$

Sol:

$$F = \overline{\{ [(\overline{A} + \overline{B}) C + D] . E + G \} H}$$

$$= \overline{(((AB+\overline{C}) . \overline{D}) + \overline{E}) \overline{G} + \overline{H}}$$ → 2 logic levels (function + input inverters)



Ex9) Redo Ex8 to obtain minimum number of T

Sol: now we will implement $\overline{F}$ & invert the output

→ the # of T = 4 T to invert A & B

+ 14T to implement the expression
+ 2 to invert the output

= 20 T

→ 20 Transistors → 3 logic levels

$\overline{F} = \overline{(((\overline{A} + \overline{B}) . C + D) . E) + G) . H}$ so implement $\overline{F}$ then invert

(to obtain the circuit schematic exchange the PMOS and NMOS blocks in the previous circuit, and invert all I/Ps, e.g. A becomes $\overline{A}$ and $\overline{C}$ becomes C)