CMOS Inverters

NMOS inverters suffered from 3 problems:

1) Reduced noise margin because :

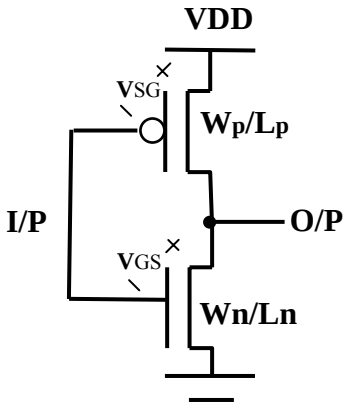
   $V_{OL} > 0$ & $V_{OH} < V_{DD}$ for (enhancement mode Load)

2) Static power dissipation when the input is high

3) Unsymmetrical T_r & T_f ($T_r >> T_f$) since we had to make $R_L >> R_{eq}$ to get V_{OL} close to 0v

The CMOS inverters solved all of these problems

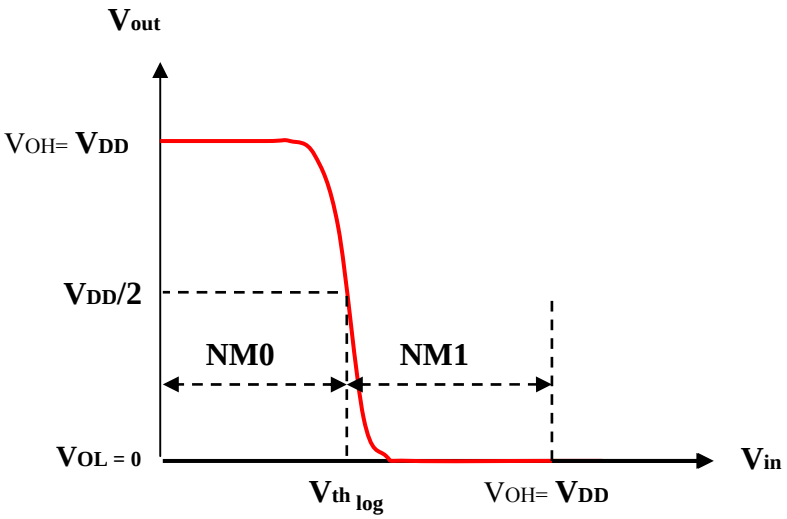
I/P	NMOS	PMOS	O/P
0v	Off	On	V_{DD}
V_{DD}	On	Off	0v



For NMOS to be ON → $V_{GS} > V_{th}$

For PMOS to be ON → $V_{SG} > V_{th}$

I = 0 (the 2 transistors are never on simultaneously → Zero static power)



Static DC characteristic

Let us find $V_{th\,log}$ where $V_{out} = V_{DD/2}$ both transistors are in saturation

$I_{SD\,PMOS} = I_{DS\,NMOS}$

$$1/2\ \mu p\, C_{ox}\ \left(\frac{Wp}{L\,min}\right)\ (V_{DD} - V_{th\,log} - |V_{tp}|)^2 = 1/2\ \mu n\, C_{ox}\ \left(\frac{Wn}{L\,min}\right)\ (V_{th\,log} - V_{th})^2$$

$$\sqrt{\frac{\mu p Wp}{\mu n Wn}}\ (V_{DD} - V_{th\,log} - |V_{tp}|) = V_{th\,log} - V_{th}$$

Assuming $V_{th} = |V_{tp}| \rightarrow$

$$V_{th\,log}\ \left(1 + \sqrt{\frac{\mu p Wp}{\mu n Wn}}\right) = (V_{DD} - V_{th})\ \left(\sqrt{\frac{\mu p Wp}{\mu n Wn}} + V_{th}\right) \rightarrow$$

$$V_{th\,log} = \frac{(V_{DD} - V_{th})\sqrt{\frac{\mu p Wp}{\mu n Wn}} + V_{th}}{1 + \sqrt{\frac{\mu p Wp}{\mu n Wn}}} = \frac{\sqrt{\frac{\mu p Wp}{\mu n Wn}}\,V_{DD} + V_{th}\left(1 + \sqrt{\frac{\mu p Wp}{\mu n Wn}}\right)}{1 + \sqrt{\frac{\mu p Wp}{\mu n Wn}}}$$

$$V_{th\,log} = \frac{\sqrt{\frac{\mu p Wp}{\mu n Wn}}\,V_{DD} + V_{th}\,\frac{1 - \sqrt{\frac{\mu p Wp}{\mu n Wn}}}{1 + \sqrt{\frac{\mu p Wp}{\mu n Wn}}}}{1 + \sqrt{\frac{\mu p Wp}{\mu n Wn}}}$$

For maximum symmetrical noise margins

to make $V_{th\,log} = V_{DD/2}$ We need to make $\sqrt{\frac{\mu p Wp}{\mu n Wn}} = 1$

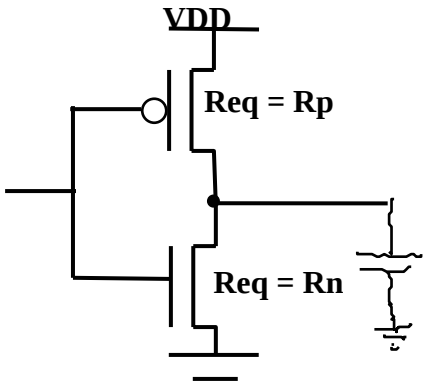
i.e $\mu p Wp = \mu n Wn$ → we know for Si $\mu n \approx 2\,\mu p$

we need to make $Wp = \frac{\mu n}{\mu p}\ Wn \rightarrow$ $Wp = 2\ Wn$

What is the relation between $V_{th\,log}$ and $\frac{Wp}{Wn}$ → Vth_{log} changes very slowly with $\frac{Wp}{Wn}$ since $V_{th\,log} \cong \frac{1}{\sqrt{\frac{Wp}{Wn}}}$

This means that noise margins are excellent and don't change much with the sizes of NMOS and PMOS

Delay of CMOS Inverters



Td ave = ½ CL (Rn + Rp)

where Rp = Req of PMOS

Rn = Req of NMOS

$$Rp = \frac{\backslash}{1/2\ \mu p\ C_{ox}\ (\frac{Wp}{L\min})\ (V_{DD} - V_{th})}$$

$$Rn = \frac{|}{1/2\ \mu n\ C_{ox}\ (\frac{Wn}{L\min})\ (V_{DD} - V_{th})}$$

The condition for symmetrical rise and fall delay is

Tr = Tf → CL Rp = C_L Rn

$$\rightarrow \mathbf{Rp = Rn} \rightarrow \frac{1}{1/2\ \mu p\ C_{ox}\ (\frac{Wp}{L\min})\ (V_{DD} - V_{th})} = \frac{1}{1/2\ \mu n\ C_{ox}\ (\frac{Wn}{L\min})\ (V_{DD} - V_{th})}$$

Assuming $V_{th} = |V_{tp}| \rightarrow \mu p Wp = \mu n Wn \rightarrow Wp = \frac{\mu n}{\mu p} Wn \rightarrow Wp = 2\ Wn$

The same conditions for equal noise margins!

Power dissipation

Static power = 0

Dynamic power $P_{dyn\ ave} = F_{I/P}\ CL\ V_{DD}^2$

Ex1 : design a CMOS inverter to operate at a maximum I/P frequency of 500 MHz at load capacitance of 100fF . use a 1 μm, 5v technology.
IDsat NMOS = 500 μA/ μm . $V_{th} = |V_{tp}| = 0.8v$

Sol : for equal NMs & Tr &Tf delays

→ Wp = 2 Wn

Td ave = 1 / (2 $F_{I/P\ max}$) = 1 / 10^9 = 10^-9 = 1 ns

= ½ CL (Rn + Rp)

Since $Wp = \frac{\mu n}{\mu p} Wn$ → Wp = 2 Wn → Rn = Rp

$T_{D\ ave} = C_L\ Rn = C_L\ Rp$

Rn = 10^(-9) / C_L = 10^ -9 \ 100x 10^-15 = 10kΩ = ($V_{DD} - V_{th}$) / ($2I_{Dsat}\ W_n$)

→ Wn = 4.2 / (1000x10^-6x10^4) = 0.42 μm

But we are using 1 μm technology → hence we set Wn = 1 μm → Wp = 2 Wn = 2 μm