WEEK 5 (LECTURES)

MOS Digital Circuits:

-Digital means ⟶ I/Ps & O/Ps are binary (0 OR 1) represented by 2 voltages: V_{OL}= (V output Low) = Logic Zero;

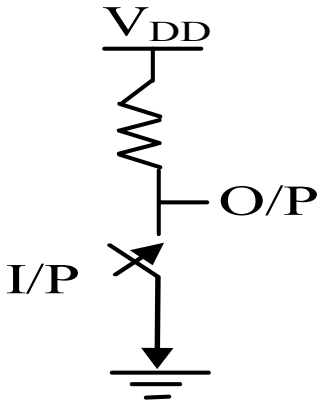
V_{OH}= (V output High) = Logic One.

-The input voltage at which the output voltage is in the middle of its range is called the logical threshold V_{thlog}.

- *How can we make Digital circuits using switches?*

1. Inverters

-Using a single NMOS switch and inverter.

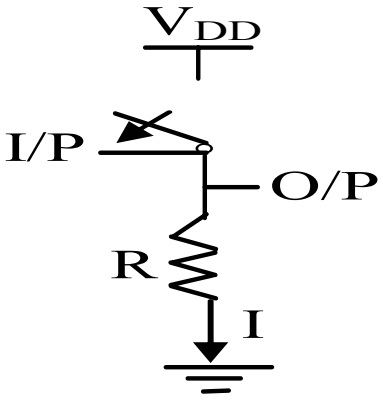


I/P	I*	V_{out}	O/P
0	0A	V_{DD}	1
V_{DD}	I	V_{DD}-IR*	0

*Where I is the current through the resistor and the NMOS switch, R is the resistance and IR is the voltage drop across the resistor

This is called NMOS inverter

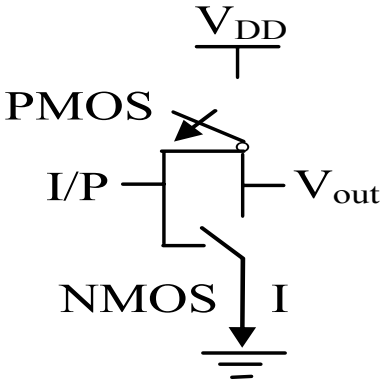
- Another way, using a single PMOS switch and a resistor:



I/P	I	V_{out}	O/P
0	I	IR	1
V_{DD}	0A	0V	0

This is called a PMOS inverter.

- ***A 3rd way using 2 switches(an NMOS and a PMOS):***



I/P	*I**	V_{out}	*O/P*
0	*0A*	V_{DD}	*1*
V_{DD}	*0A*	*0V*	*0*
**I is the current through the two switches*			

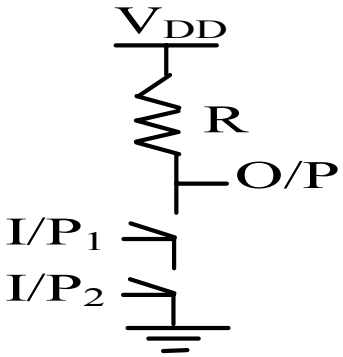
This is called CMOS (Complementary MOS) inverter.

Other gates;

ex. 2 I/P NAND?

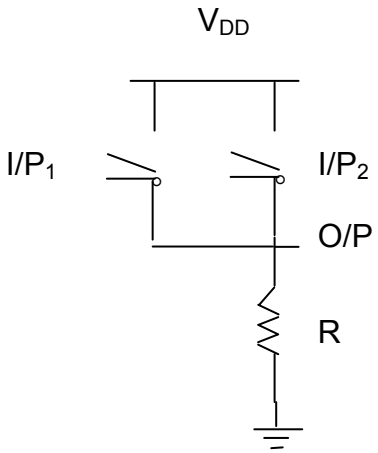
- ***NMOS NAND:***

  O/P = 0 only If both I/P are 1 & O/P =1 otherwise

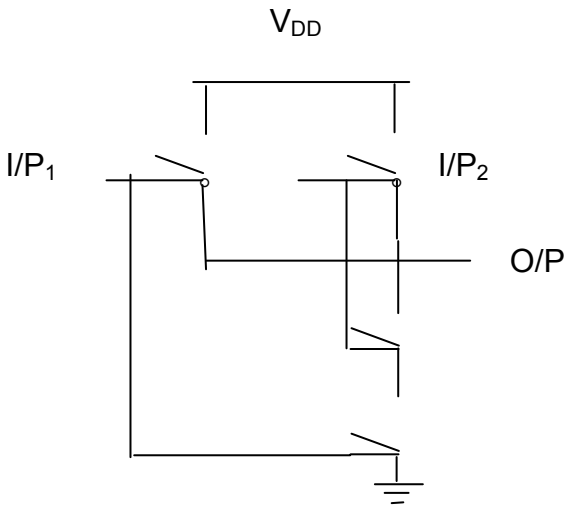


I/P_1	I/P_2	*O/P*
0	*0*	*1*
0	*1*	*1*
1	*0*	*1*
1	*1*	*0*

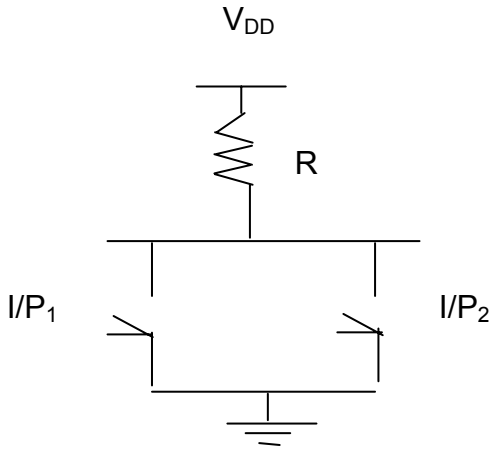
- ***PMOS NAND:***



- ***CMOS NAND:***

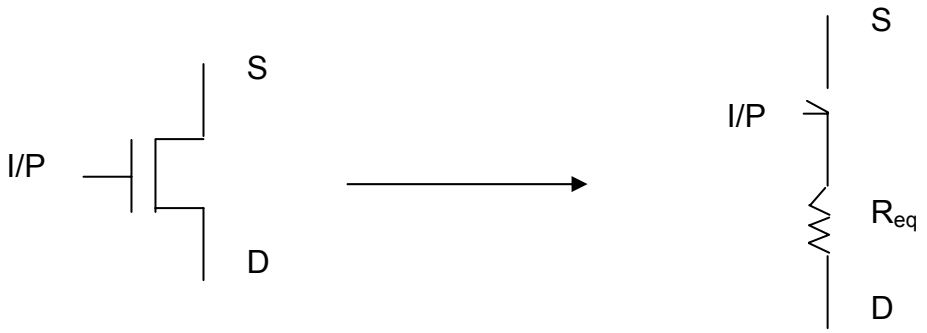


- ***NMOS 2 I/P NOR:***

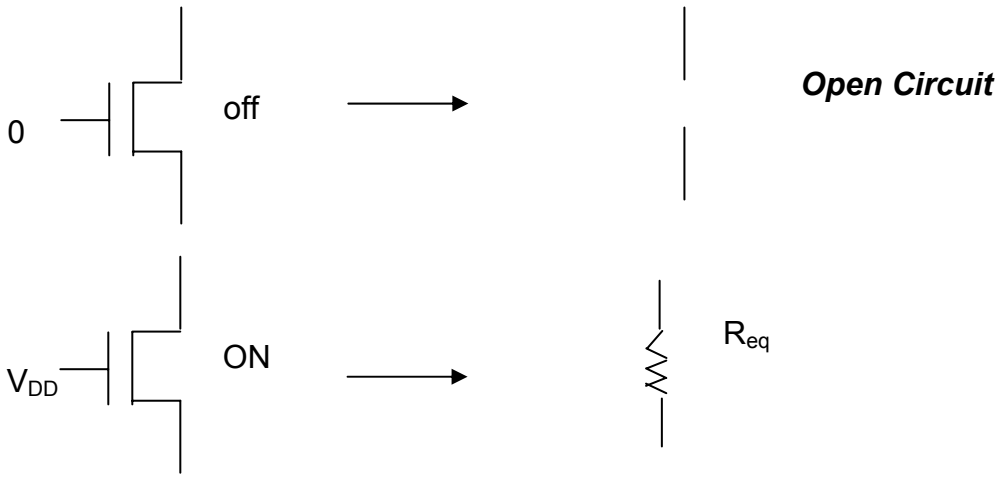


Modeling The MOSFET as a Switch:

We will utilize the fact that in digital circuits all transistors will have either a 1 or 0 input to simplify the way we do calculations. So transistors are either ON or OFF. Hence we can model them as shown below:



- ***We model the NMOS switch (or the PMOS switch) as an ideal switch in series with a resistance.***
- ***The ideal switch has no voltage drop across it when it is ON or closed and is an open circuit when it is OFF or open.***
- ***This means that the transistor is Open Circuit when OFF (zero current through it) and has a resistance R_{eq} when it is ON (I/P = V_{OH})***



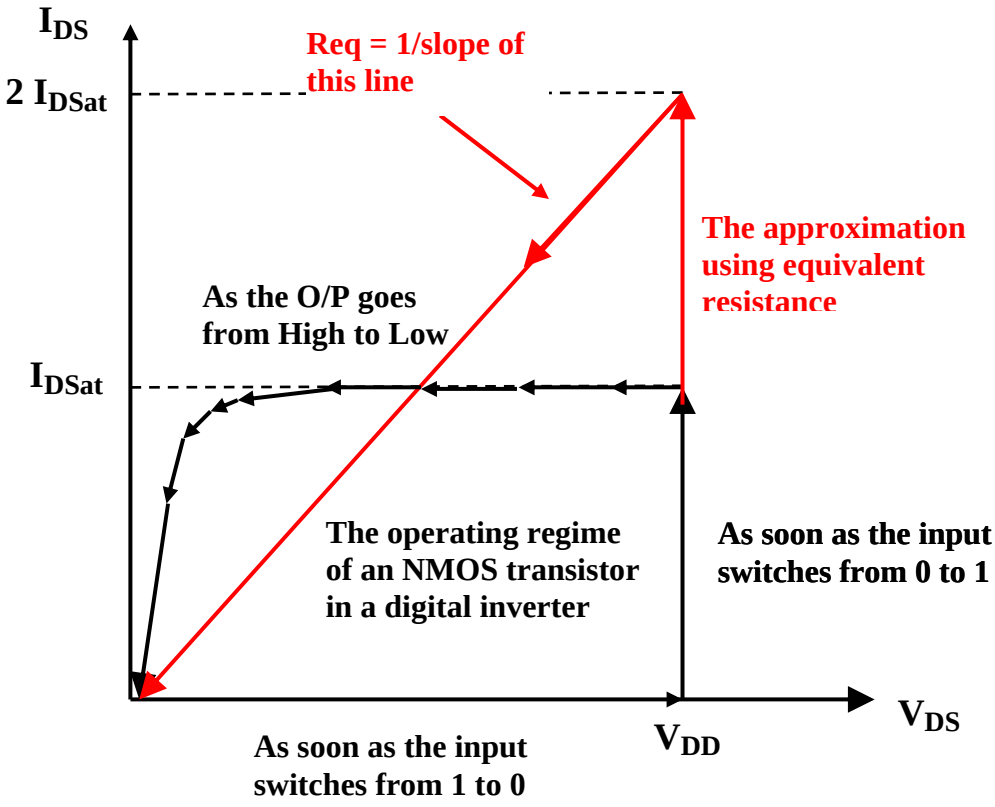
R_{eq}= the resistance of the MOS channel in the ON state.

We will approximate this resistance as (see the graph below):

R_{eq}= V_{DD}/ 2I_{Dsat}

I_{Dsat} (@ $V_{DS} = V_{GS} = V_{DD}$) = ½ M_n C_{ox} (w/L) $(V_{DD} - V_{th})^2$

$R_{eq} = V_{DD} / M_n C_{ox} (w/L) (V_{DD} - V_{th})^2 = 1 / M_n C_{ox} (w/L) (V_{DD} - V_{th})$



- *Usually IC manufacturers provide designers with device parameters such as L_{min}, V_{DD}, V_{th}, C_{ox} & $I_{Dsat/\mu m}$.*

$I_{Dsat/Mm} = I_{DS}$ *with* $L = L_{min}$, $w = 1$ µm, $V_{DS} = V_{GS} = V_{DD}$

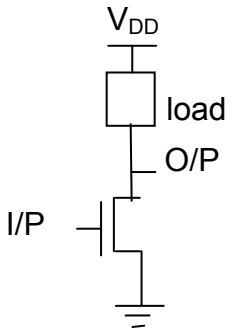
→ R_{eq} *of a MOSFET with width w:*

$$R_{eq} = (V_{DD} - V_{th}) / (2\, I_{Dsat/\mu m} * w)$$

$$= 1 / (\mu_n C_{ox} (w/L_{min}) (V_{DD} - V_{th}))$$

NMOS Inverter:

Basic structure



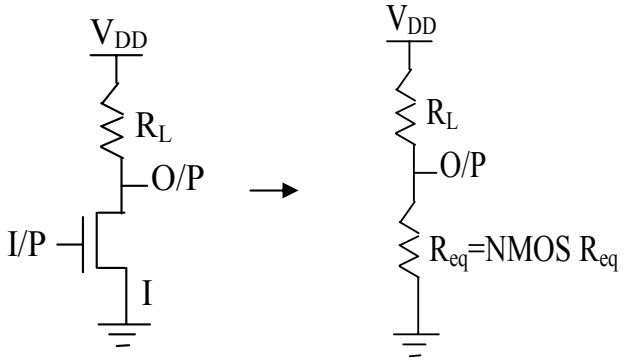
The load is always ON

⟶ ***3 types are possible depending on the load:***

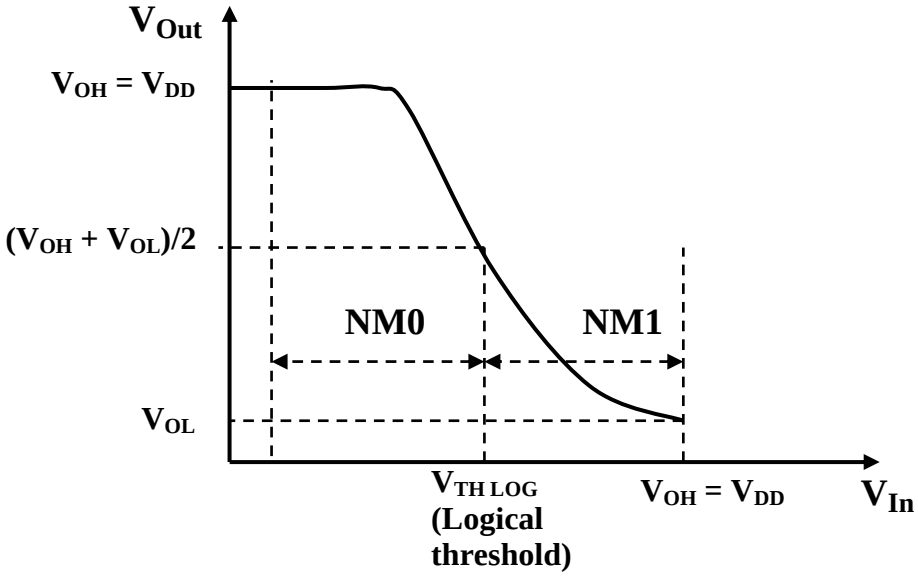
1- Resistive Load:

$$V_{OH} = V_{DD}$$

$$V_{OL} = V_{DD} - IR = (V_{DD} * R_{eq}) / (R_{eq} + R_L)$$



-Voltage Characteristics and noise margins:



→ ***Average static Power:***

$$P_{DCaverage} = \frac{1}{2} V_{DD} I = \frac{1}{2} (V_{DD}^2 / (R_{eq} + R_L))$$

Noise Margins (NMs):

NMs can be approximated as:

$$NMO = V_{thlog} - V_{OL}$$

$$NM1 = V_{OH} - V_{thlog}$$

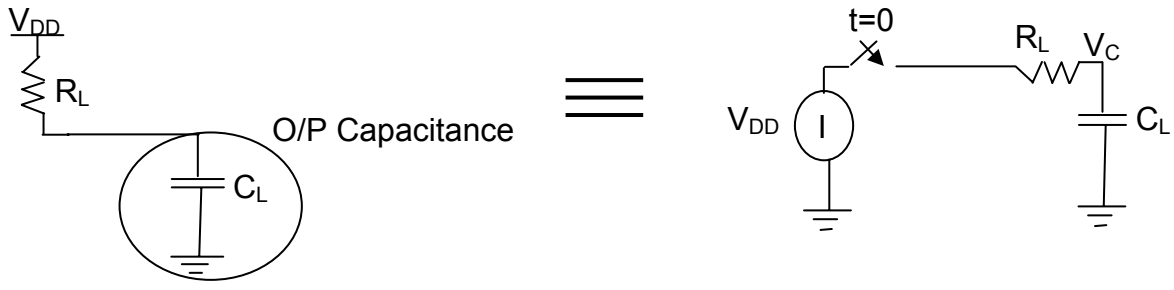
Average Propagation Delay:

When I/P = V_{OL}

The rising Delay T_r = time From I/P = 50% of its final value to rising O/P reaching 50% of its final value (≈ 0.5 V_{DD})

T_r is approximated as $R_L C_L$

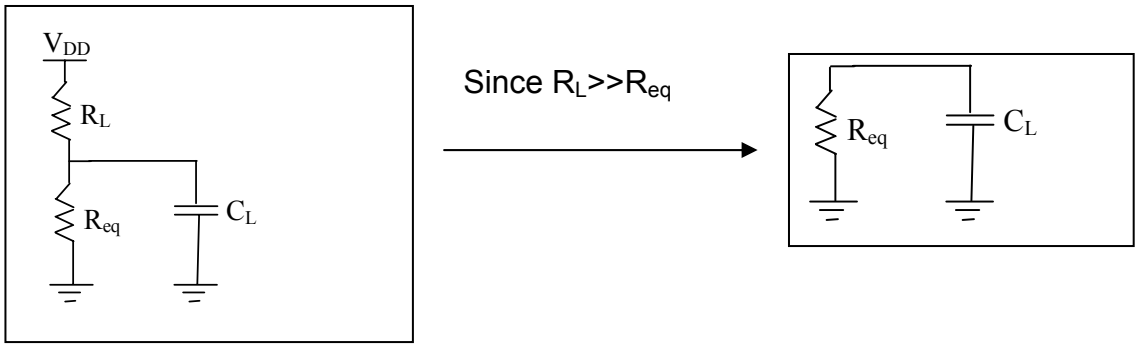
This is obtained as follows: We are charging the output capacitance C_L through a resistance R_L as shown in the figure below. Hence



$$V_C(t) = V_{DD}(1 - \exp(-t / R_L C_L))$$

$$@\ t = R_L C_L;\quad V_C = V_{DD}(1 - \exp(-1)) = 0.69\, V_{DD} \approx 0.5\, V_{DD}$$

Fall Delay T_f = time From I/P = 50% of its final value
to falling O/P reaching 50% of its final value (≈ 0.5 V_{DD})



$T_f = R_{eq}\ C_L$

$\therefore T_{Dave}$ *(average Prob. Delay)* $= ½\ (T_f + T_r) = ½\ C_L\ (R_L + R_{eq})$

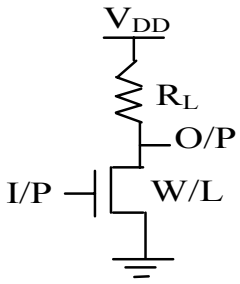
⟶ *The max. possible I/P freq. :* $F_{I/Pmax} = 1/2T_{Dave}$

⟶ *Dynamic Power:* $P_{Dynave} = F_{I/P}\ C_L\ V_{DD}^2$

Ex. ***Design an NMOS inverter with the following specifications*** $V_{OH} = V_{DD}$; $V_{OL} = 0.1\ _{VDD}$; $P_{DCave} = 10$µw. Assume a (1µm, 5V) technology, $I_{Dsat/Mm(NMOS)}$ = 500µA/µm & V_{th} =0.8V.

Ans.

1. Circuit



2. Using resistive load:

$V_{OH} = V_{DD}$

$V_{OL} = (V_{DD}\ R_{eq})/(R_{eq} + R_L) = 0.1V_{DD}$

⟶ $R_{eq} = 0.1(R_L + R_{eq})$ → $R_L = 9\ R_{eq}$ ---------- 1

→ $P_{DCave} = 10*10^{-6} = ½ (V_{DD}^2 / (R_{eq} + R_L))$

→ $R_L + R_{eq} = 12.5/10*10^{-6} = 1.25MΩ$ ---------- 2

→ Sub. 1 in 2:

$10\ R_{eq} = 1.25*10^6$ R_{eq} → $= 0.125\ MΩ = 125\ KΩ$

→ $R_L = 9*125\ KΩ = 1.125\ MΩ$

For the NMOS assuming $L = L_{min}$

$R_{eq} = (V_{DD} - V_{th})/2\ I_{Dsat/Mm} * w$ →

$w = 4.2/2*500*10^{-6}*125*10^3 = 0.034\ \mu m$

However we are using a 1 μm technology → This means nothing can be less than 1 μm.

→ This w was calculated assuming $L = L_{min} = 1\ \mu m$

→ The required w/L = 0.034/1 , let w =1 μm

→ $1/L = 0.034$ → $L = 1/0.034 = 30\ \mu m$

Ex. For the inverter design in last example, calculate the noise margins & maximum I/P freq. at a load of 100ff ($100*10^{-15}F$).

Ans.

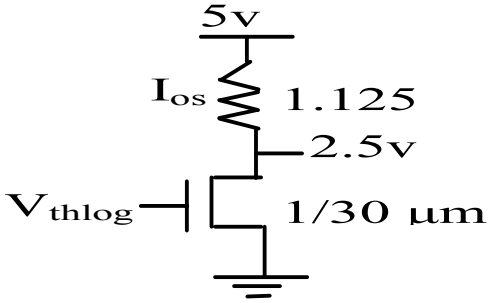
$NM0 \approx V_{thlog} - V_{OL}$

$NM1 \approx V_{OH} - V_{thlog}$

V_{thlog} (logical + threshold) is the input voltage that would make $V_{out} \approx V_{DD}/2$.

In this case:

Assuming that the NMOS is in saturation:



$I_{DS} = (V_{DD} - (V_{DD}/2))/R_L = 2.5/1.125\ MΩ$

$= 2.22*(10^{-6}) = ½ M_n C_{ox} (w/L)(V_{GS} – Vth)^2$

$= ½ \mu_n C_{ox} (w/L)(Vthlog – Vth)^2$

To find $\mu_n C_{ox}$, we use $I_{Dsat/\mu m}$ given in example.

$I_{Dsat/Mm} = 500\mu A = ½ \mu_n C_{ox} (1/1)(V_{DD} – V_{th})^2$

$\longrightarrow \mu_n C_{ox} = (100*10^{-6})/4.2^2$

Sub. In 1:

$2.22*10^{-6} = ½ ((1000*10^{-6})/(4.2^2))*0.034 (V_{thlog} – 0.8)^2$

$\sqrt{((4.44*4.2^2)/34)} = (V_{thlog} – 0.8)$

$\longrightarrow V_{thlog} = 2.318V \longrightarrow V_{GS} = 2.318 < 2.5 = V_{DS}$

$\longrightarrow$ So, our assumption was correct.

$\therefore NM0 = 2.318 – 0.5 = 1.818V$

$NM1 = 5 – 2.318 = 2.692V$

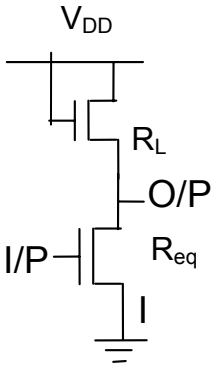
$F_{I/Pmax} = 1/2T_{Dave} = 1/(T_r + T_f)$

$\longrightarrow T_r = C_L*R_L = 100ff*1.125*10^6 = 112.5ns$

$\longrightarrow T_f = C_L*R_{eq} = 100ff*125K\Omega = 12.5ns$

$\longrightarrow F_{I/Pmax} = 1/125ns = 8MHz$

2- Enhancement NMOS Load:



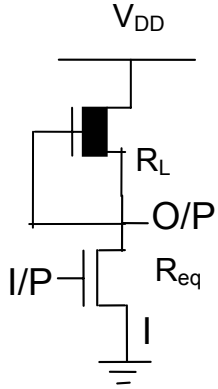
$V_{OH} = V_{DD} – V_{th}$

$V_{OL} = V_{DD} (R_L/(R_L + R_{eq}))$

R_L: equivalent resistance of the load transistor.

(Reduced noise margins, but smaller area than the resistive load)

3- Depletion NMOS Load:



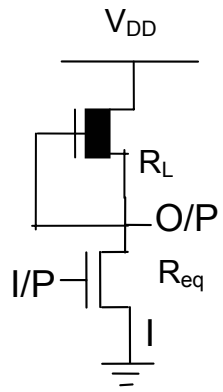
The depletion load has $V_{th} < o$

$V_{OH} = V_{DD}$

$V_{OL} = V_{DD} (R_L/(R_L + R_{eq}))$

$\longrightarrow P_{DCave} = ½ (V_{DD}^2)/(R_L + R_{eq})$

EX. ***Design a depletion load NMOS inverter such that V_{OL} = $0.1V_{DD}$ P_{DCave} = $10\mathcal{M}$ W.Use the $1\mathcal{M}$m, 5V technology. Assume Vth for the depletion NMOS = -2V.***



Ans.

$V_{OH} = 5V = V_{DD}$

$V_{OL} = V_{out}$ *when* $V_{in} = 5V$

The driver NMOS is in linear region

The load NMOS is in sat.

$I_{DSload} = I_{DSdriver}$ →

$$\tfrac{1}{2}\,\mu_n C_{ox}\,(w/L)_L\,(0-(-2))^2 = \mu_n C_{ox}\,(w/L)_D\,((5-0.8)0.5 - \tfrac{1}{2}\,(0.5)^2)$$

⟶ $(W/L)_L = 0.49\,(w/L)_D$ ----------1

Also, $P_{DCave} = 10*10^{-6} = 0.49/2$ @ $V_{in} = V_{OH}*V_{DD}$

→ I_{DS} *when* $V_{in} = 5V = 20*10^{-6}/5 = 4\mu A$

$= \tfrac{1}{2}\,\mu_n C_{ox}\,(w/L)_L\,(4)$ → *this gives us* $(w/L)_L$ *and then from 1 we get* $(w/L)_D$