COE360 Course Project (022)
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Choose one of the following projects depending on your group size. For all projects use AMI's 0.5 µm technology (5V supply) and assume 2 pF load capacitance at all your circuit's outputs. Also, all gates should have symmetrical noise margins

I. **Projects for Groups of 3:**

1. Design an 8-bit Shift and Add multiplier capable of 50 MOPS.
2. Design a 6-bit pipelined parallel multiplier with a clock frequency of 800 MHz.

II. **Projects for Groups of 2:**

3. Design a 16-bit Adder/Accumulator with an output left/right shift capability and operating frequency of 250 MHz.
4. Design a circuit that counts the occurrence of a certain pattern in an input bit stream. The pattern is 5-bit long (10101). The circuit should be resetable and able to count up to 255 patterns at an input bit frequency of 500 Mbps.
5. Design an 8-bit X 8 FIFO buffer that can be read and written simultaneously with an operating frequency of 500 MHz.

The deliverables for this project are as follows:

1. **Phase I: Logic Design** **Due Monday 19/2/1424 (21/4/2003)**

   This is the gate level implementation of the Adder. This part should include logic verification (e.g. using Logic Works or HDL).

2. **Phase II: Circuit Design** **Due Saturday 9/3/1424 (10/5/2003)**

   This is the transistor level implementation of the adder. This part includes all the SPICE files simulation results.

3. **Phase III: Mask Design (layout)** **Due Wednesday 4/4/1424 (4/6/2003)**

   This is the physical mask level (i.e. layout) implementation of the adder. It includes the post-layout verification using IRsim and SPICE simulations. All layouts should be DRC clean and clearly labeled. A short final report documenting the whole project should be submitted and an exit interview shall be conducted.