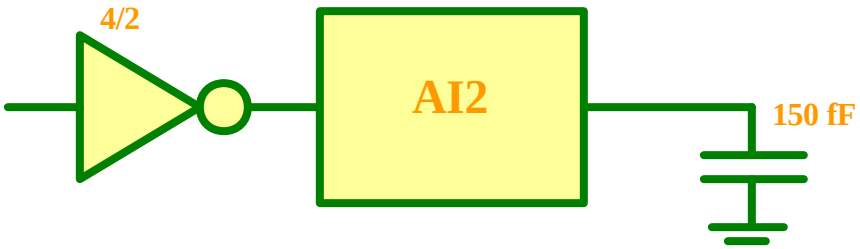
COE 360 – 6th Assignment/Quiz – Dr. Muhammad Elrabaa

1. **Using Spice, obtain the optimum P/N ratio (PMOS width to NMOS width) for a CMOS AI2 gate. Assume the total load capacitance is 150 fF and that an inverter with a P/N ratio of 4µm/2µm is driving the AI2 gate. Use the AMI 0.5µm, 5V technology. You should size the AI2 gate such that the total delay from the inverter's input to the AI2 output is minimum. Also measure the average dynamic power at an input switching frequency of 200 MHz.**



2. **Obtain a layout of the AI2 gate using Magic and the SCMOS technology.**