COE360 – Assignment # 4 (Out of 20)
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For this assignment, use WinSpice and the AMI0.5 µm technology. You can get WinSpice from my shared folder \\coe-elrabaa\sharedFolder\IC Design Resources\WinSpice or from the internet. There are 2 example Spice files on my website; one for DC analysis and another for transient analysis (do not forget to use the appropriate technology though!).

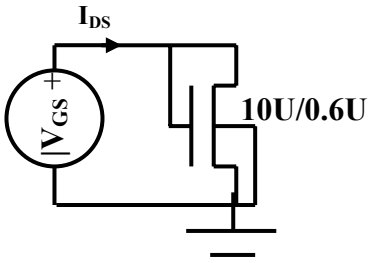
Q1) Use SPICE to find the following parameters of the 0.5 µm technology:

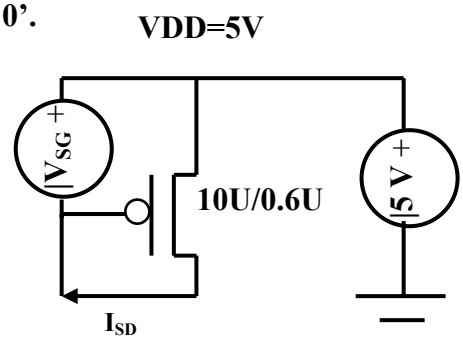
Vtn, Vtp, $I_{DSat(NMOS)}$/µm and $I_{SDsat(PMOS)}$/µm

Hint: Use a single NMOS and a single PMOS circuits. Do a DC sweep on VGS (for NMOS) and VSG (for PMOS) with the drain connected to the gate to find Vth (when the device starts to turn on) and I_{DSat} (I_{DS} when VGS=VDS=VDD=5V). Divide the current you get by 10 to get I_{DSat}/µm

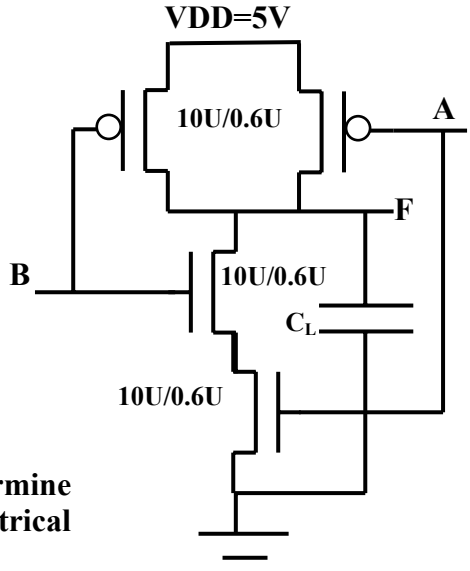
Note that the substrate of the NMOS is always connected to the lowest voltage where that of the PMOS is connected to the highest voltage.

I_{DS} the can be measured by plotting '–I(V_{GS})/10'.





Q2) For the circuit shown below:



1. **Using operating point analysis verify that this is a NAND gate (when AB=00, 01, or 10 F=1 and when AB=11, F=0)**

2. **Using DC sweep, fixing A at 5V and sweeping B from 0 to 5 V, plot the voltage characteristics Of this gate (Vout versus Vin) and determine V_{OL}, V_{OH}, V_{IL}, V_{IH}, $V_{Thlogical}$ (logical threshold) , NML and NMH**

3. **Keeping the PMOS transistors at the same size, And varying the NMOS sizes use DC sweep to determine the size ratio PMOS to NMOS that will give symmetrical noise margins (i.e. 2.5V logical threshold)**

4. **With a load capacitance (C_L) of 100 fF and keeping the size Ratio between the PMOS and NMOS sizes as in 3 find the NMOS and PMOS sizes that will give an average delay of 100 pS (i.e. 10^{-10} seconds). Always keep L at the minimum value of 0.6 µm**