**COE360 – Assignment # 5 (out of 20)**
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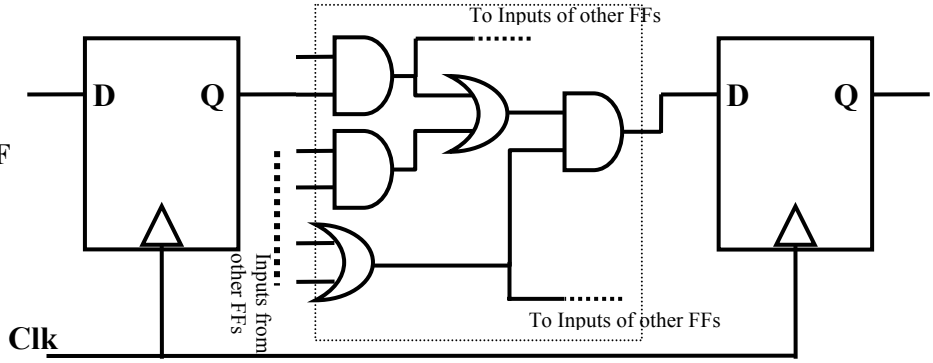
**In all the questions below, whenever is required assume the following: a 1 µm technology with $V_{DD}$=5V, $C_{ox}$=2 fF/µm$^2$, $\epsilon_{rox}$= 4, $\epsilon_{rSi}$= 12, $\epsilon_o$= 8.85E-14 F/cm, $\mu_n$=600 cm$^2$/S·V, $\mu_p$=250 cm$^2$/S·V, $I_{Dsat_{nmos}}$= 500 µA/µm, $I_{Dsat_{pmos}}$= 200 µA/µm, $V_{tn} = |V_{tn}|$ = 0.8 V, and q=1.6E-19 C.**

**Q1) Implement the following function in CMOS using minimum number of transistors and show the symbolic layout:**

$$F = (A + \overline{B}) \cdot C + D \cdot E$$

**Q2) The circuit below is to operate at a clock frequency of 2 GHz (i.e. 0.5 nS cycle time). The D-FFs are to have the following parameters:**

$C_{in}$ (D input)= 100 fF
$T_{setup}$ = 75 pS
$T_{hold}$ = 50 pS
$T_{CK \rightarrow Q}$ = 125 pS




1. **Determine the required delay of the combinational logic (inside dotted box) for the 2 GHz operation.**

2. **Design the circuit (including the FFs) to achieve the required delay with minimum number of devices, minimum overall area, equal path delays (i.e. the delay from any input to the output is the same) and equal noise margins.**

**Q2) Design a non-inverting (i.e. with even number of stages) CMOS buffer chain with an input capacitance of 35 fF to drive a load of 3.5 pF with minimum delay and equal noise margins and rise and fall delays.**