COE 561 Digital System Design and Synthesis, Term 071
Assignment # 5, Due Sunday, January13th, 2008

Q.1. Consider the incompletely-specified FSM represented by the following state table:

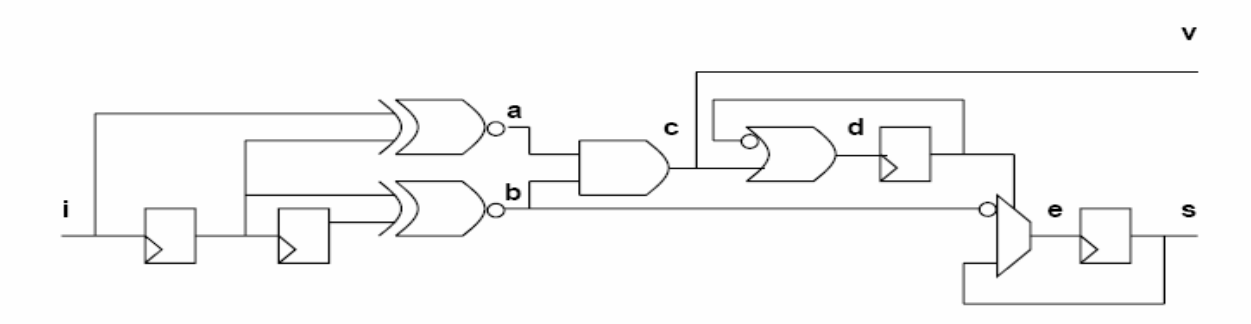
Input	Present State	Next State	Output
0	S1	S1	0
1	S1	S4	*
0	S2	S2	0
1	S2	S1	1
0	S3	S4	0
1	S3	S5	1
0	S4	S6	0
1	S4	S5	1
0	S5	S6	1
1	S5	S1	0
0	S6	S3	*
1	S6	S5	1

(i) Replace the don't-care conditions by 0's and minimize the obtained state stable.

(ii) Replace the don't-care conditions by 1's and minimize the obtained state stable.

(iii) Minimize the state table of the incompletely specified FSM.

Q.2. Consider the synchronous sequential circuit given below-specified FSM represented by the following state table:



(i) Draw the synchronous network graph corresponding to the given circuit. In the graph, vertices represent inputs, outputs, gates, and fanout stems.

(ii) Assume that delay of each gate is 1. Retime the graph to reduce the cycle time. Draw the resulting circuit.

(iii) Read the library **synch.genlib** using the command **read_library synch.genlib**. Then, map your design to the library using the command **map –s**. Then, retime the circuit using the command **retime**. Compare the maximum arrival time before and after retiming. Compare the obtained solution to the solution you obtained in (ii).

Q.3. Solve problems 4.1 and 4.2 in the text book.