Proposal for COE 485 (Automation and VLSI #1)

Project Title : Design and Synthesis of Digital Systems using Synopsys and FPGA tools

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Overall Objectives :

The project involves the design and synthesis of digital systems for different application areas covering processor architecture, networking, multimedia, etc. using Synopsys and Xilinx FPGA tools.

Major Tasks

The project involves the following major tasks :
A] Hardware modeling of a selected system using hardware description language, VHDL
B] Synthesis of the system using Synopsys tools
C] Implementation by mapping the design onto Xilinx FPGAs

Project requirements

- Study of a Hardware Description Language – VHDL
- Study of Synopsys synthesis tools
- Study of Xilinx FPGA tools
- Literature survey on the topics selected

Pre-requisite : Senior Standing
Desirable : Design experience using VHDL or Verilog
Duration : One/Two semesters

Project Deliverables

- Prototype on a FPGA board
- User/Technical Document containing details on the design, analysis, coding, simulation, synthesis and FPGA mapping.
- Demonstration of the working model
- Two Presentations (Midterm & Final)

List of Projects

- ## Project 1

Title : **VHDL Modeling and FPGA implementation of 10/100Mbps Ethernet MAC**

Brief Description :

This project involves the modeling of a 10/100 Mbps Ethernet MAC using VHDL, synthesizing the design using Synopsys tools and implementation of the resulting design using Xilinx FPGAs. Ethernet MAC is a part of Ethernet device which controls the transmission and reception of data packets based on CSMA/CD protocol. 10/100Mbps Ethernet MAC consists of two parts, the Transmitter and the Receiver. In OSI communication model, Ethernet MAC is included in the data link layer.

The 10/100 Mbps Ethernet MAC performs the following main functions :

- Establishing connection between physical layer and network layer during data transfer process.
- Packeting data using 802.3 standard data packet format.
- Preamble generation and removal.
- Collision detection using CSMA/CD protocol
- Detecting error in received data packet.
- Automatic 32-bit CRC generation and checking.
- Controlling data flow in Ethernet NIC

No. of students : **One/Two**

- **Project 2**

Title : **VHDL Modeling and FPGA implementation of 100 BASE-T4 Network Repeater**

Brief Description :

This project involves the modeling of a 100 BASE-T4 Network repeater using VHDL, synthesizing the design using Synopsys tools and implementation of the resulting design using Xilinx FPGAs. The basic function of a repeater is to retransmit data that is received from one port to all other ports. 100BAE-T4 is the 100 Mbps Ethernet standard that operates over four pairs of category 3, 4, or 5 UTP cable.

The basic objectives for a repeater are to :

- Detect carrier activity on ports and receive Ethernet frames on active ports
- Restore the shape, amplitude, and timing of the received frame signals prior to transmission
- Forward the Ethernet frame to each of the active ports
- Detect and signal a collision event throughout of the network
- Extend a network's physical dimensions
- Protect a network from failures of stations, cables, ports and so forth.
- Allow the installation and removal of stations without network disruption
- Partition bad segments

The project involves the following main tasks :

- Study of the architecture of a 100 BASE-T4 repeater
- Designing the Repeater core logic

No. of students : **Two**

- # Project 3

Title : **VHDL Modeling and FPGA implementation of a Worm-Hole Router**

Brief Description :

This project involves the modeling of a Worm-hole Router using VHDL, synthesizing the design using Synopsys tools and implementation of the resulting design using Xilinx FPGAs. A router is required to control the flow of information between processors and interconnection network. Each processor divides messages into units called packets before sending. Transmission of each packet follows a technique called worm-hole routing where the sections of a packet, flits, flow through the network in a pipelined fashion. A pipelined wormhole router architecture can provide high and predictable performance for integrated traffic in clusters.

The major tasks to be performed in this project are :

- Detailed study of Worm-hole Router architecture (literature survey)
- Implementation
- Performance evaluation

No. of students : **Two**

- # Project 4

Title : **VHDL Modeling and FPGA implementation of a Floating point processor for Custom Computing Machines**

Brief Description :

Image and digital signal processing applications typically require high calculation throughput. Many algorithms rely on floating point arithmetic for the dynamic range of representations and require millions of calculations per second. Such computationally intensive algorithms are candidates for acceleration using custom computing machines(CCMs) being tailored for the application. Unfortunately, floating point operators require excessive area (or time) for conventional implementations. Instead, custom formats, derived for individual applications are feasible on CCMs and can be implemented on a fraction of a single FPGA. Using hardware description languages, like VHDL facilitates the development of custom operators without significantly impacting operator performance or area. This project involves the modeling of a floating-point processor using VHDL, synthesizing the design using Synopsys tools and implementation of the resulting design using Xilinx FPGAs. Area consumption and speed of working arithmetic operators used in real time applications are also to be taken into account.

The major tasks to be performed in this project are :

- Design and implementation of
    - floating point adder
    - floating point subtractor
    - floating point multiplier
    - floating point divider
- Performance evaluation in terms of CLBs and Routing delays

No. of students : **Two**

- # Project 5
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Title : **VHDL Modeling and FPGA implementation of a High Speed Multipliers**

Brief Description :

This project involves the modeling of various high speed multipliers using VHDL, synthesizing the design using Synopsys tools and implementation of the resulting design using Xilinx FPGAs. These multipliers find extensive use in Image/video processing applications.

The major tasks to be performed in this project are :

- Detailed study of various high speed multiplication algorithms(literature survey)
- Implementation of these algorithms.
- Performance evaluation

No. of students : **One**

- # Project 6

Title : **VHDL Modeling and FPGA implementation of a CORDIC chip**

Brief Description :

This project involves the modeling of a CORDIC chip using VHDL, synthesizing the design using Synopsys tools and implementation of the resulting design using Xilinx FPGAs. CORDIC is a set of shift-add algorithms for computing a wide range of functions including certain trigonometric, hyperbolic, linear and logarithmic functions. These algorithms find extensive use in Digital signal processing applications.

The major tasks to be performed in this project are :

- Detailed study of various CORDIC algorithms(literature survey)
- Implementation of these algorithms.
- Performance evaluation

No. of students : **Two**