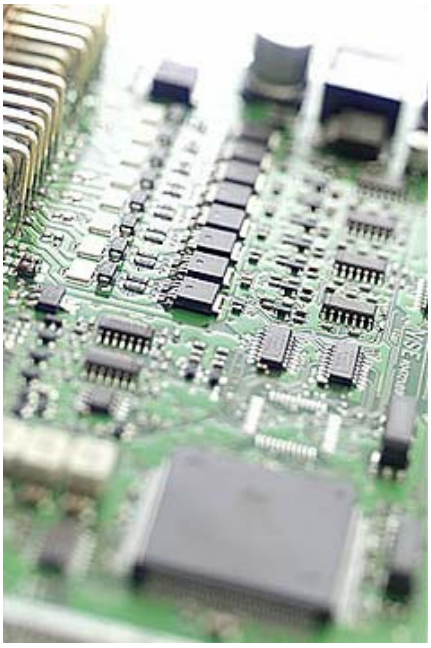
King Fahd University of Petroleum and Minerals
College of Computer Sciences & Engineering
Computer Engineering Department

COE 360: CMOS Digital Integrated Circuits

Serial to Parallel Converter Project



Advisor: Dr. M. ELrabaa

Done By:
Abdullah H. Al-Qhatani 206012
Khaled M. Al-Dossari 226910

Abstract:

This report is containing the phase one for designing a simple serial-to-parallel data converter. The report will be divided into five parts. The first part will be the introduction about the project and the way to implement it. The second part will be the Data Unit designing. The third part will be about the Control Unit and how to implement it. The fourth part will be the testing and simulation about the design. In the last part, the problems faced and the conclusion about the designing and implementation of the circuit will be mentioned.

The Report Contents

CHAPTER I

INTRODUCTION

INTRODUCTION:

This is the phase one for designing a simple serial-to-parallel data converter.

Project Description:

The circuit reads data serially, adds a parity bit to it and then output it in parallel (8-bits) along with a strobe signal. The data format is as follows; 2 start bits (two 1s), a single stop bit (0) and the data packets (each is 7-bits long) are separated by a single 1 (continuation bit). When there is no data on the input it is kept low (i.e. 0). The circuit will be fully synchronous with an external clock and have a master asynchronous reset input.

Project Implementation:

The project is divided into two parts Data Unit and Control Unit. The Data Unit is consists of Four parts:

- Parity Test
- 7-Bit Shift Register
- 8-Bit Load Register
- 3-Bit Counter

The Control Unit has two flip flops to select the state and outputs four signals to control the Data Unit and those signals are:

- Load signal
- Count signal
- Clear signal
- Shift signal

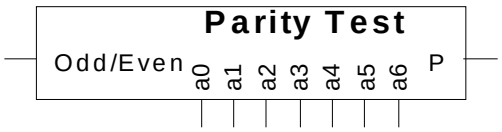
CHAPTER II

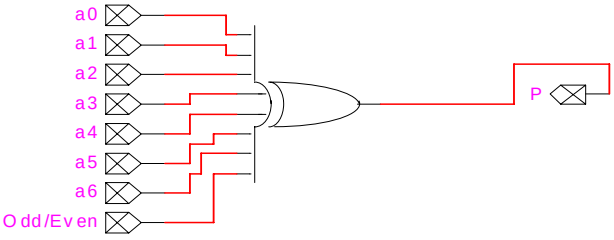
THE DATA UNIT

A. Parity Generator:

Objective:

The purpose of this circuit is to generate the parity bit from the 7-bits input from the serial port with the Odd/Even party input.

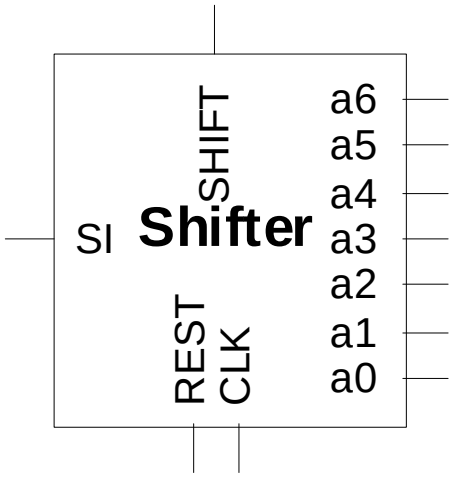


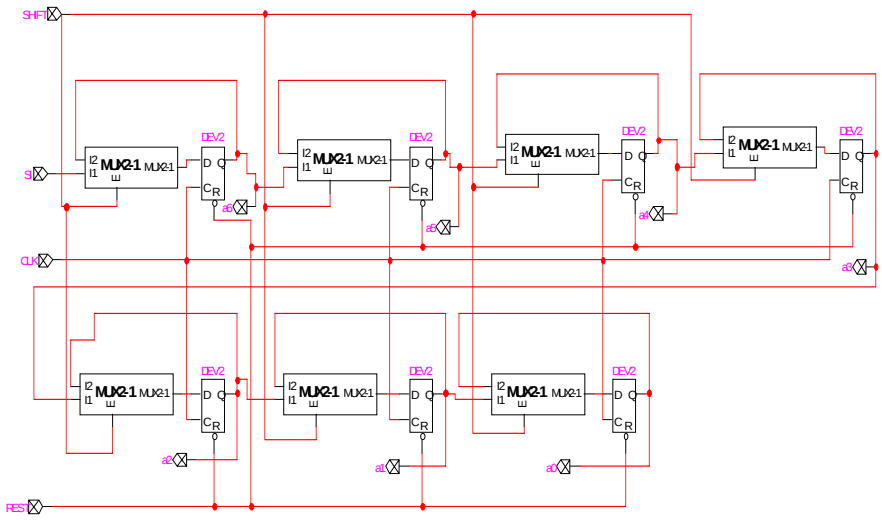


B. 7-Bit Shift Register:

Objective:

The purpose of this circuit is to shift 7-BITS input from the serial port (packet) and this circuit is controlled by shift signal from the Control Unit.

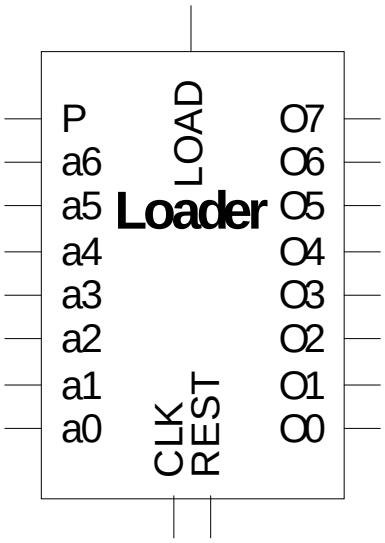


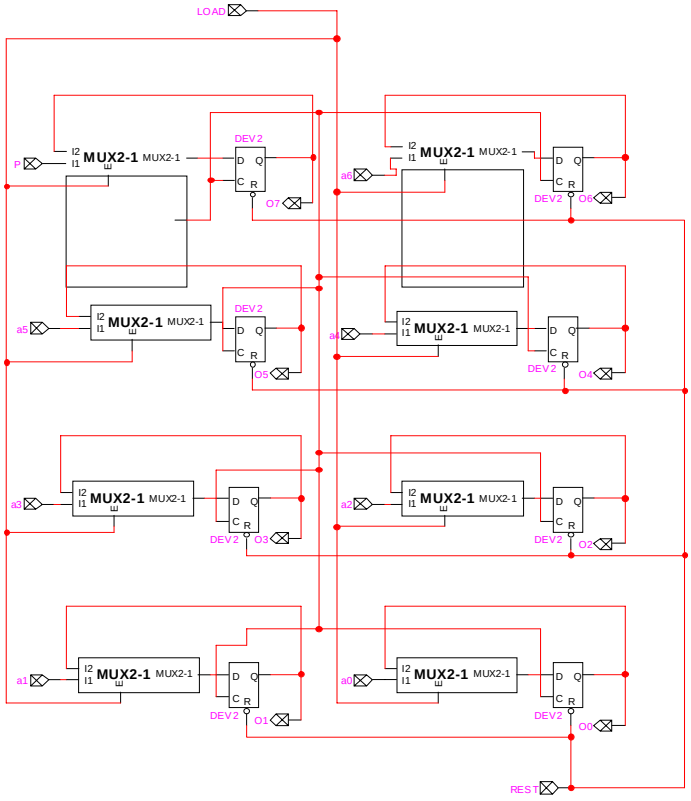


C. 8-Bit Load Register:

Objective:

The purpose of this circuit is to load the 7-BITs in the shift resisters in additional to the party bit when the load signal coming from the Control Unit.

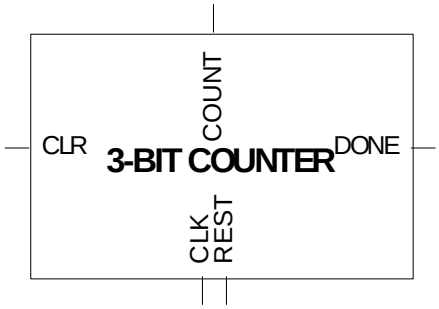


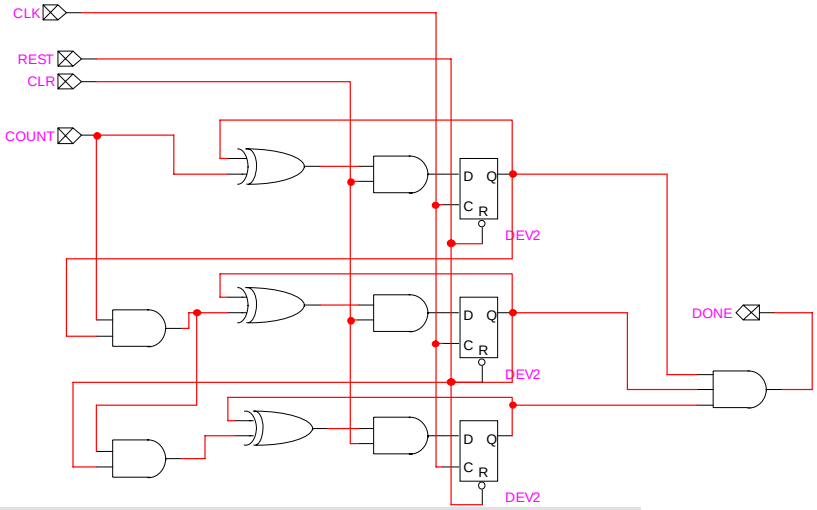


D. 3-Bit Counter:

Objective:

The purpose of this circuit is to count up to 7 and generate a DONE signal when the count finished. It is controlled by a count signal to start counting and clear signal to clear the counter.

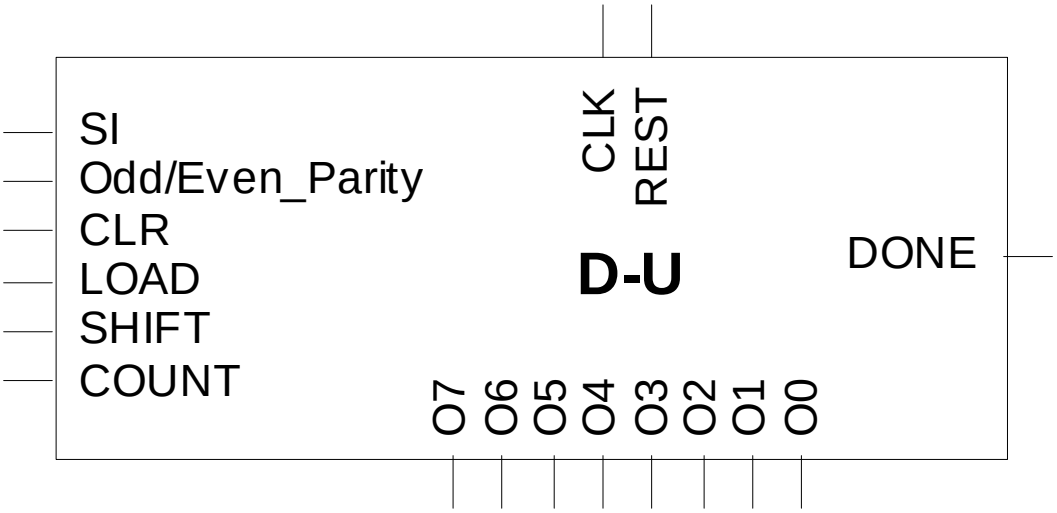


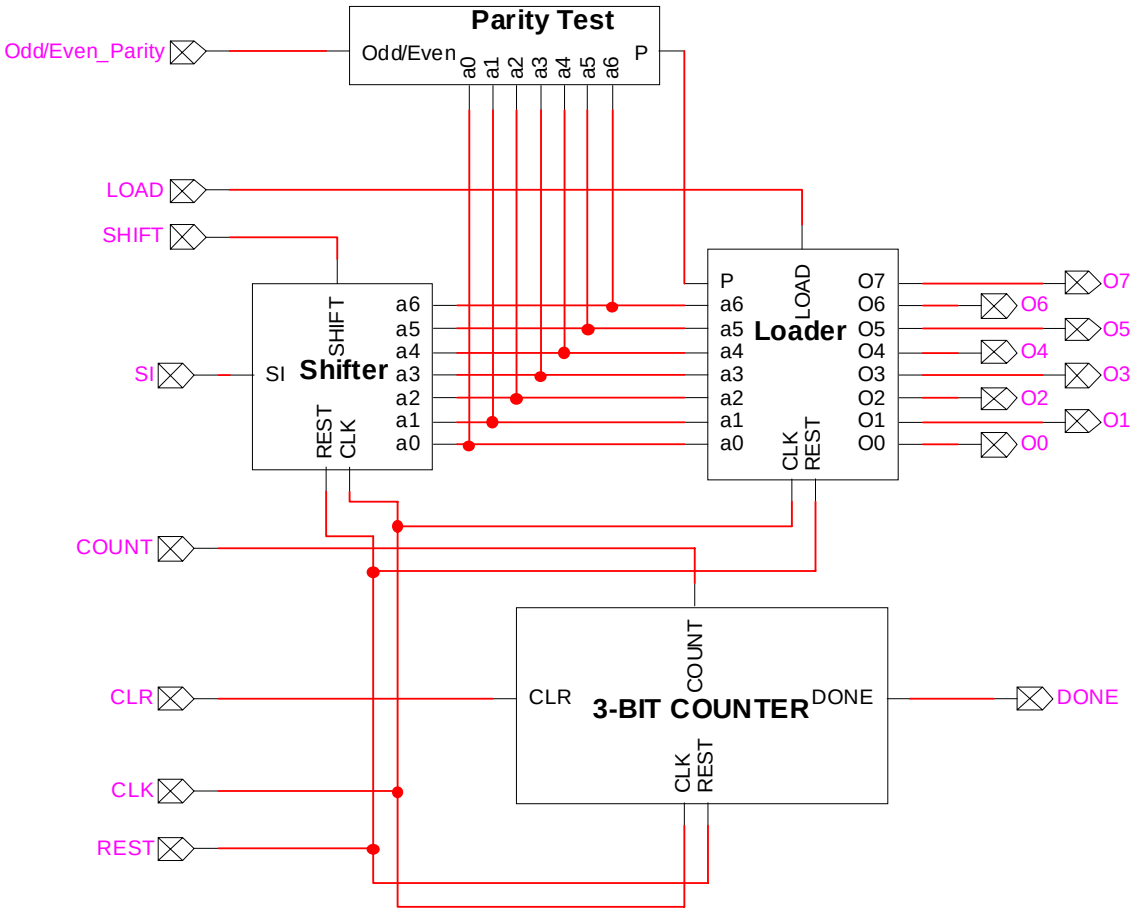


Data Unit:

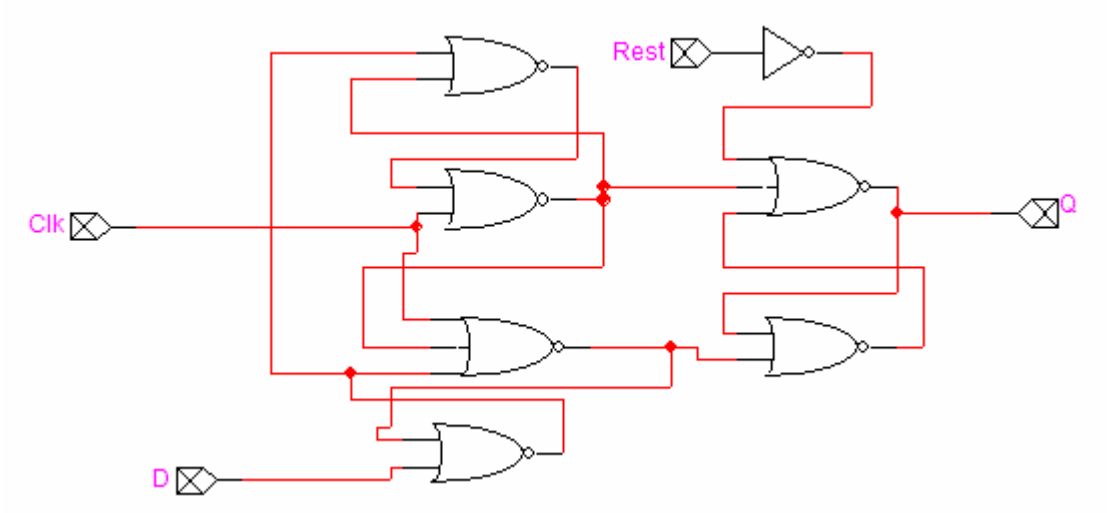
Objective:

This unit consists of the parity test, 7-bit shift register, 3-bit counter and 8-bit loader registers. It takes its input from the control unit and serial input (SI). It outputs the packet content and DONE signal.

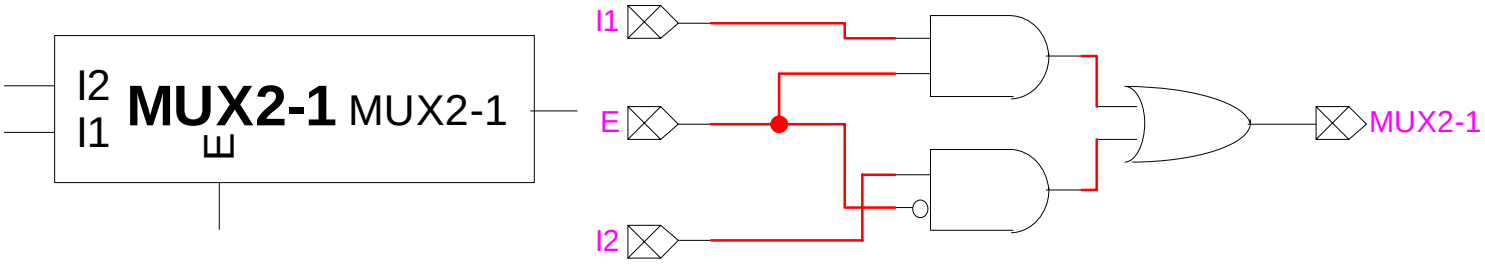




Flip Flop Design:



Multiplexer:

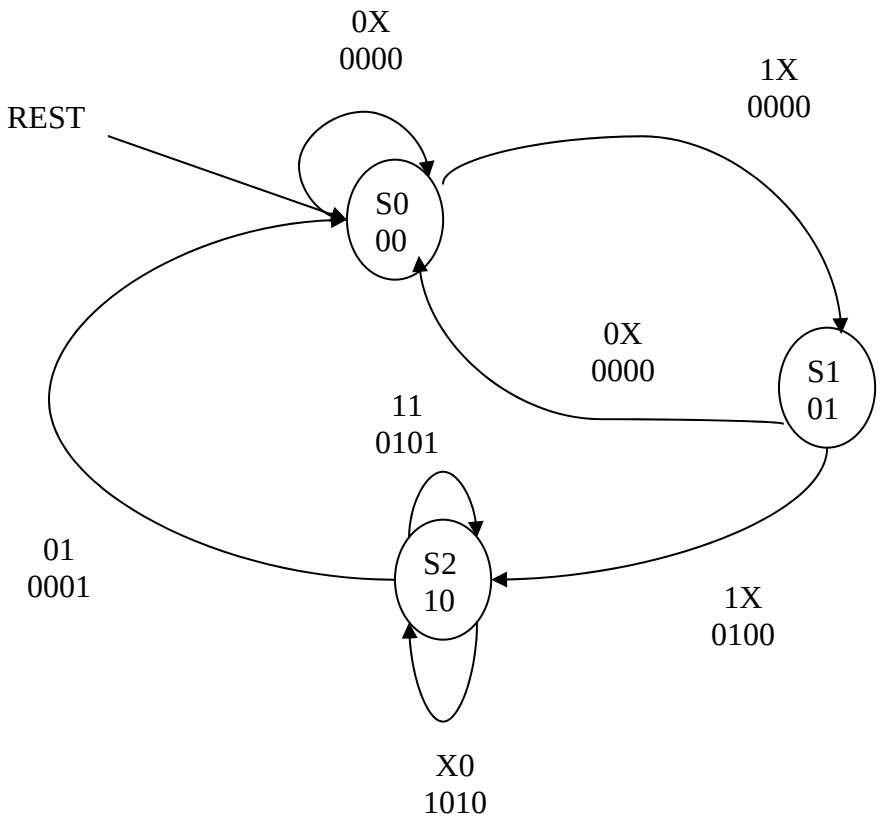


CHAPTER III

THE CONTROL UNIT

STATE Diagram:

INPUT	SI	DONE		
OUTPUT	COUNT	CLR	SHIFT	LOAD/STRB



Control Unit Truth Table:

P. STATE		INPUT		N. STATE		OUTPUT			
DA	DB	SI	DONE	QA	QB	COUNT	CLR	SHIFT	LOAD
0	0	0	X	0	0	0	0	0	0
0	0	1	X	0	1	0	0	0	0
0	1	0	X	0	0	0	0	0	0
0	1	1	X	1	0	0	1	0	0
1	0	X	0	1	0	1	0	1	0
1	0	1	1	1	0	0	1	0	1
1	0	0	1	0	0	0	0	0	1
1	1	X	X	0	0	0	0	0	0

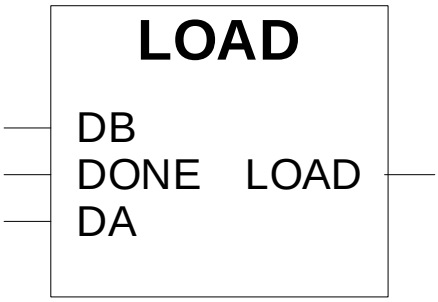
A. Load signal:

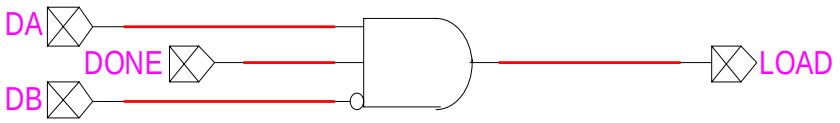
Objective:

It is used to control the 8-bit loader when the packet is ready.

DA DB\SI DONE	00	01	11	10
00				
01				
11				
10		1	1	

LOAD=DA.DB'.DONE





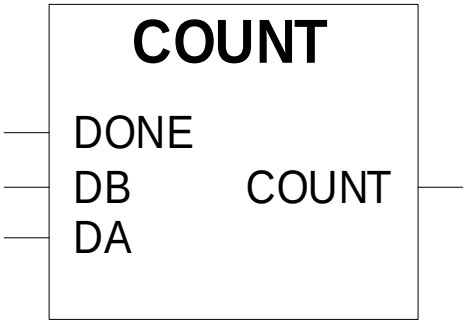
B. Count Signal:

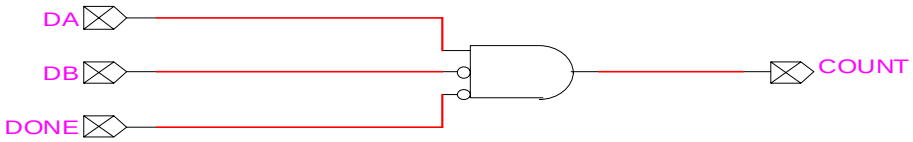
Objective:

It is used to control the 3-bit counter when 2 start bits are received.

DA DB\SI DONE	00	01	11	10
00				
01				
11				
10	1			1

COUNT=DA.DB'.DONE'





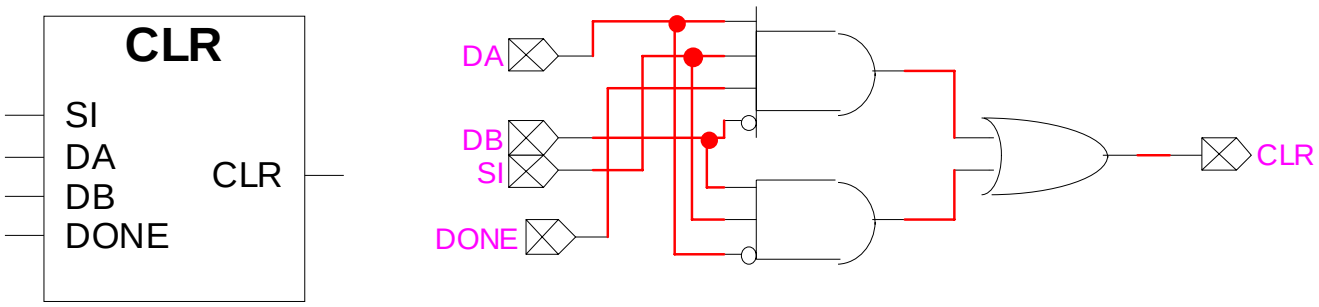
C. Clear signal:

Objective:

It is used to clear the content of the counter after finishing the count.

DA DB\SI DONE	00	01	11	10
00				
01			1	1
11				
10			1	

CLR=DA'. DB.SI+DA. DB'. SI. DONE



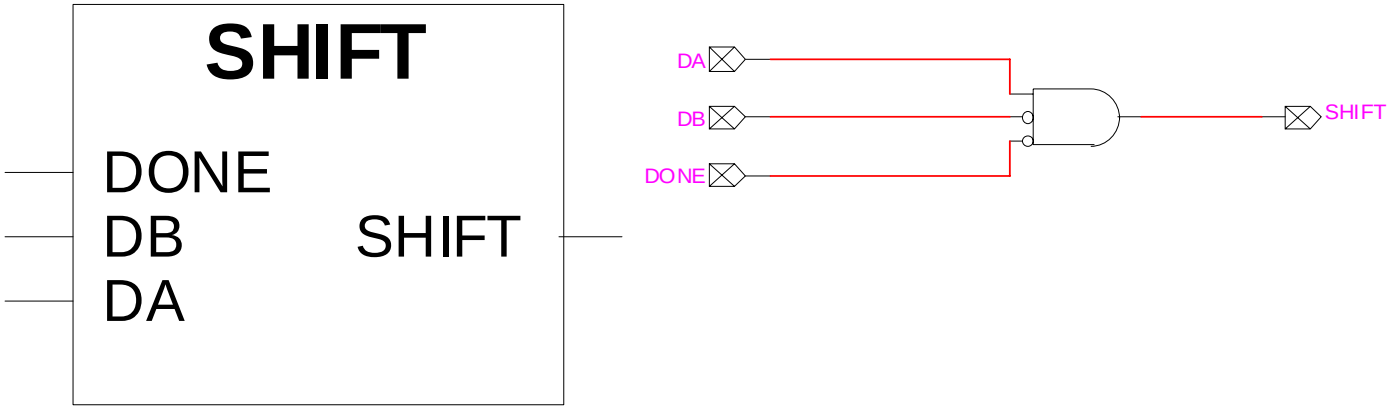
D. Shift signal:

Objective:

It is used to control the 7-bit shifter when the first bit of the packet is received.

DA DB\SI DONE	00	01	11	10
00				
01				
11				
10	1			1

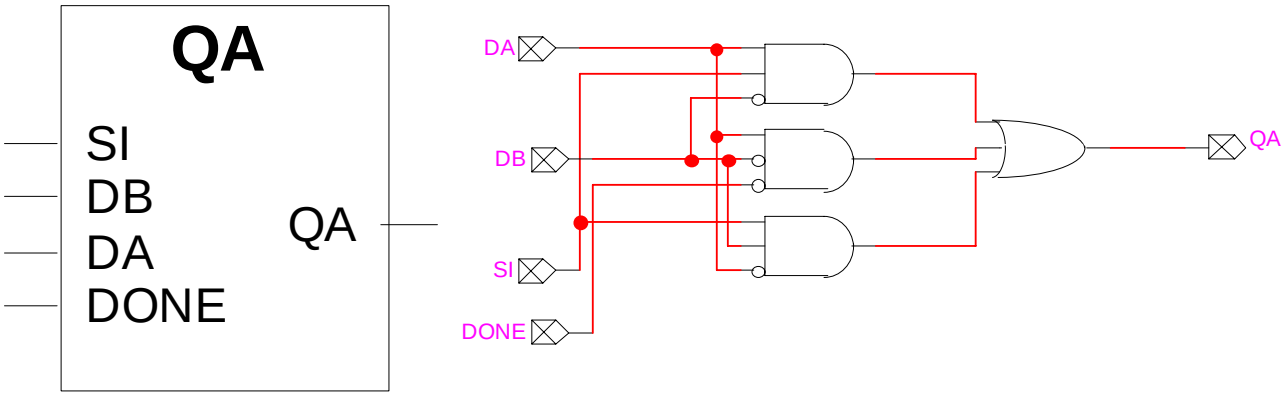
SHIFT=DA.DB’.DONE’



E. QA (Next State):

DA DB\SI DONE	00	01	11	10
00				
01			1	1
11				
10	1		1	1

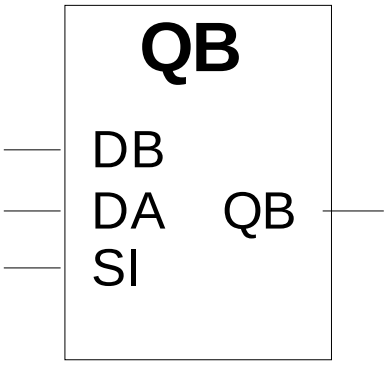
QA=DA.DB’.SI. + DA.DB’.DONE’. +DA’DB.SI

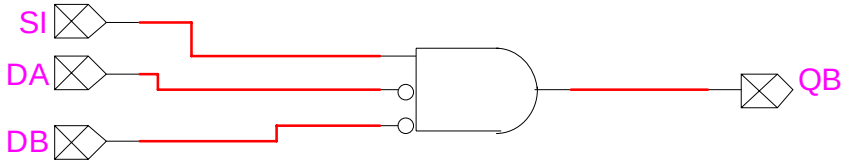


F. QB (Next State):

DA DB\SI DONE	00	01	11	10
00			1	1
01				
11				
10				

QB=DA'.DB'.SI

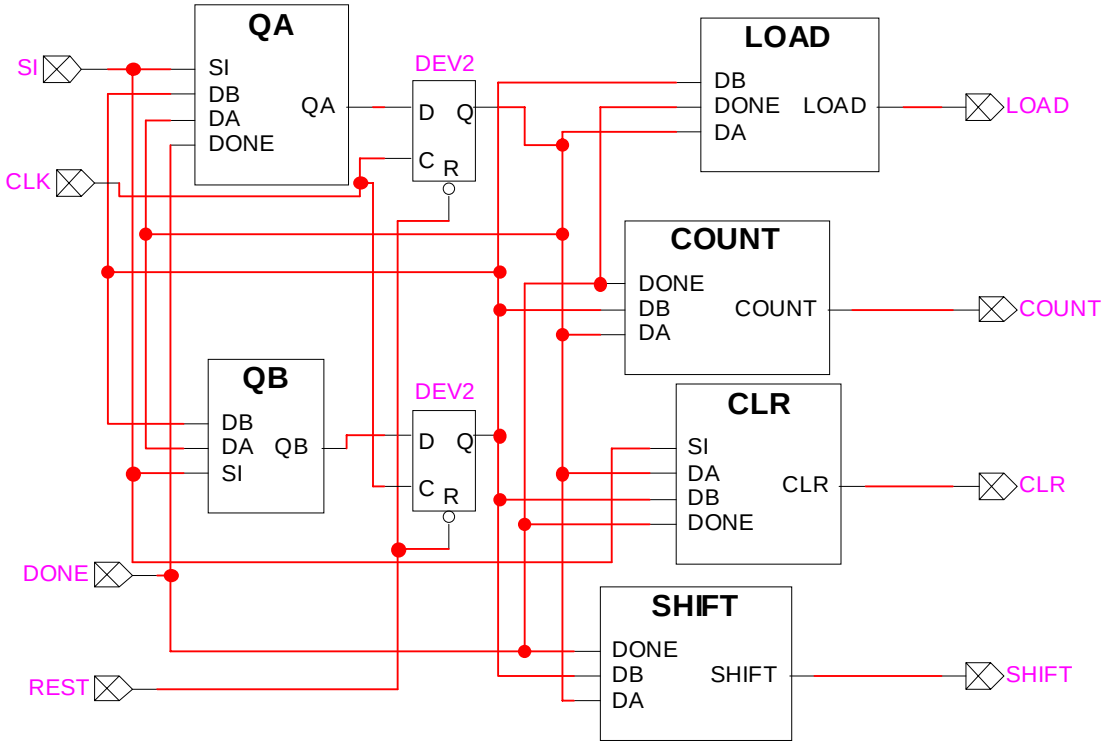


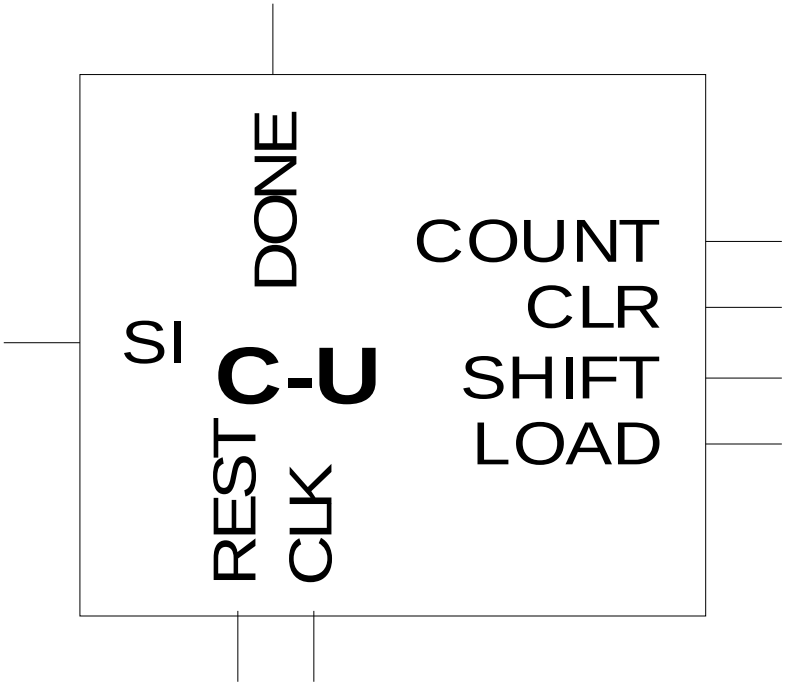


Control Unit:

Objective:

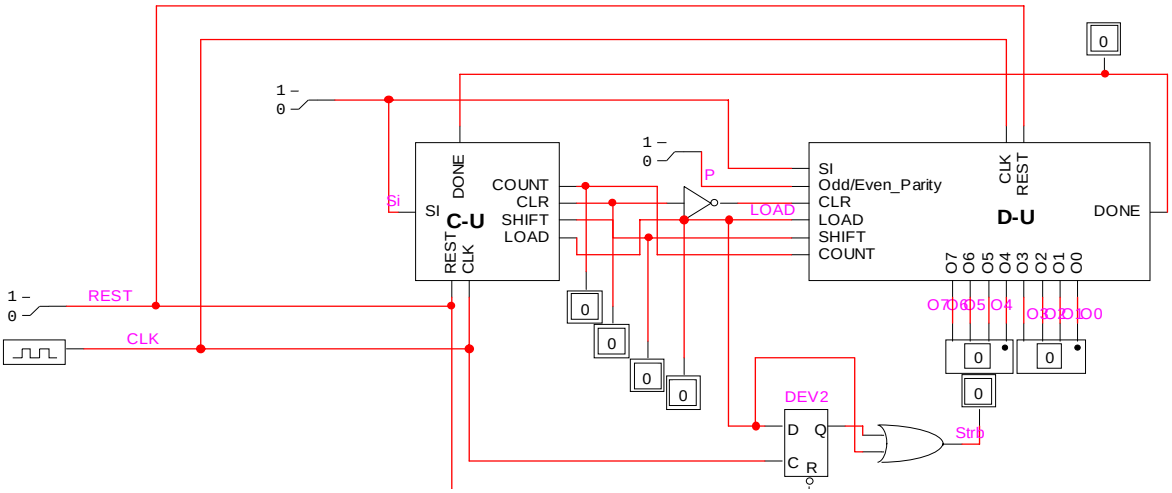
It controls the data unit by giving the LOAD, SHIFT, COUNT and CLEAR.



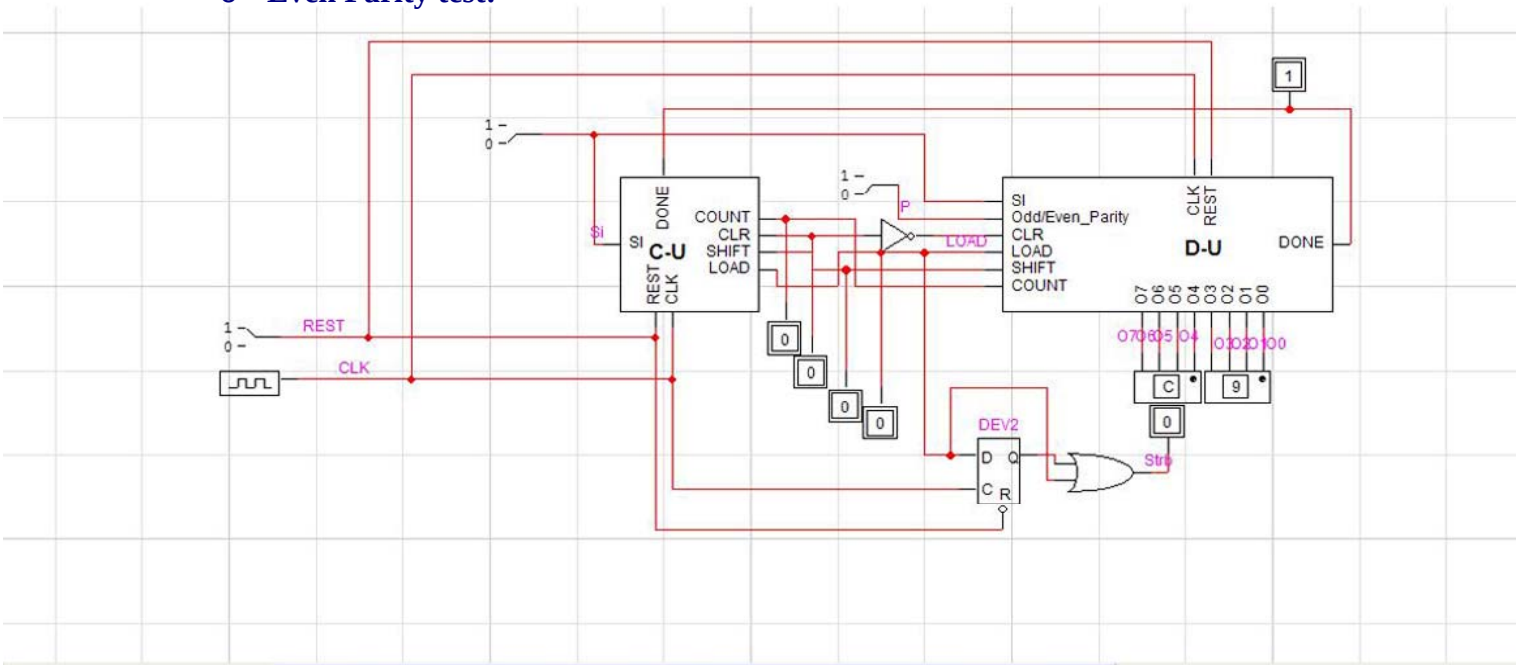


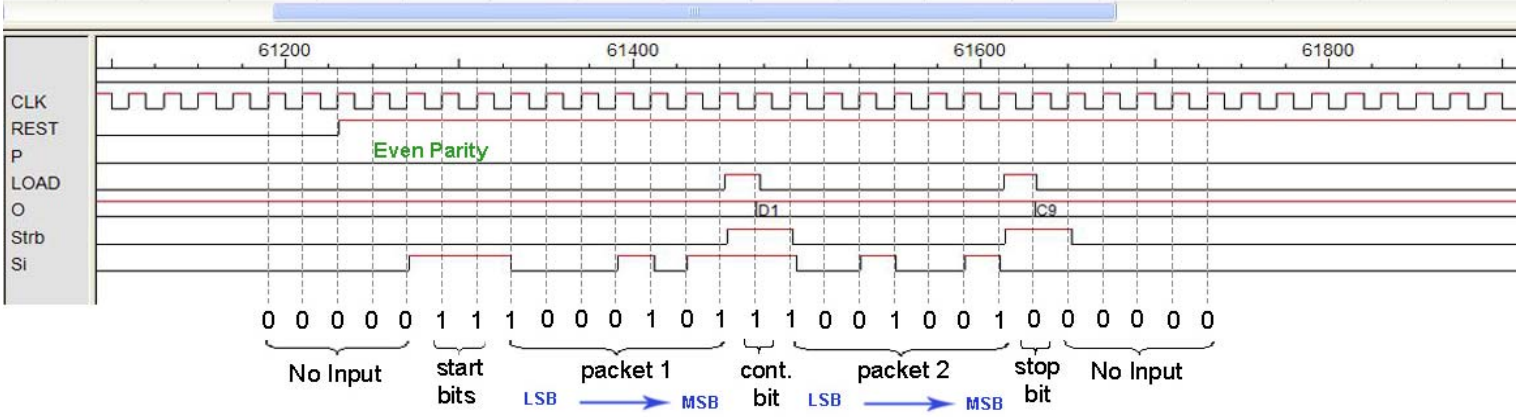
CHAPTER IV
TESTING AND SIMULATION

- **This is the final circuit which we made the testing on it.**

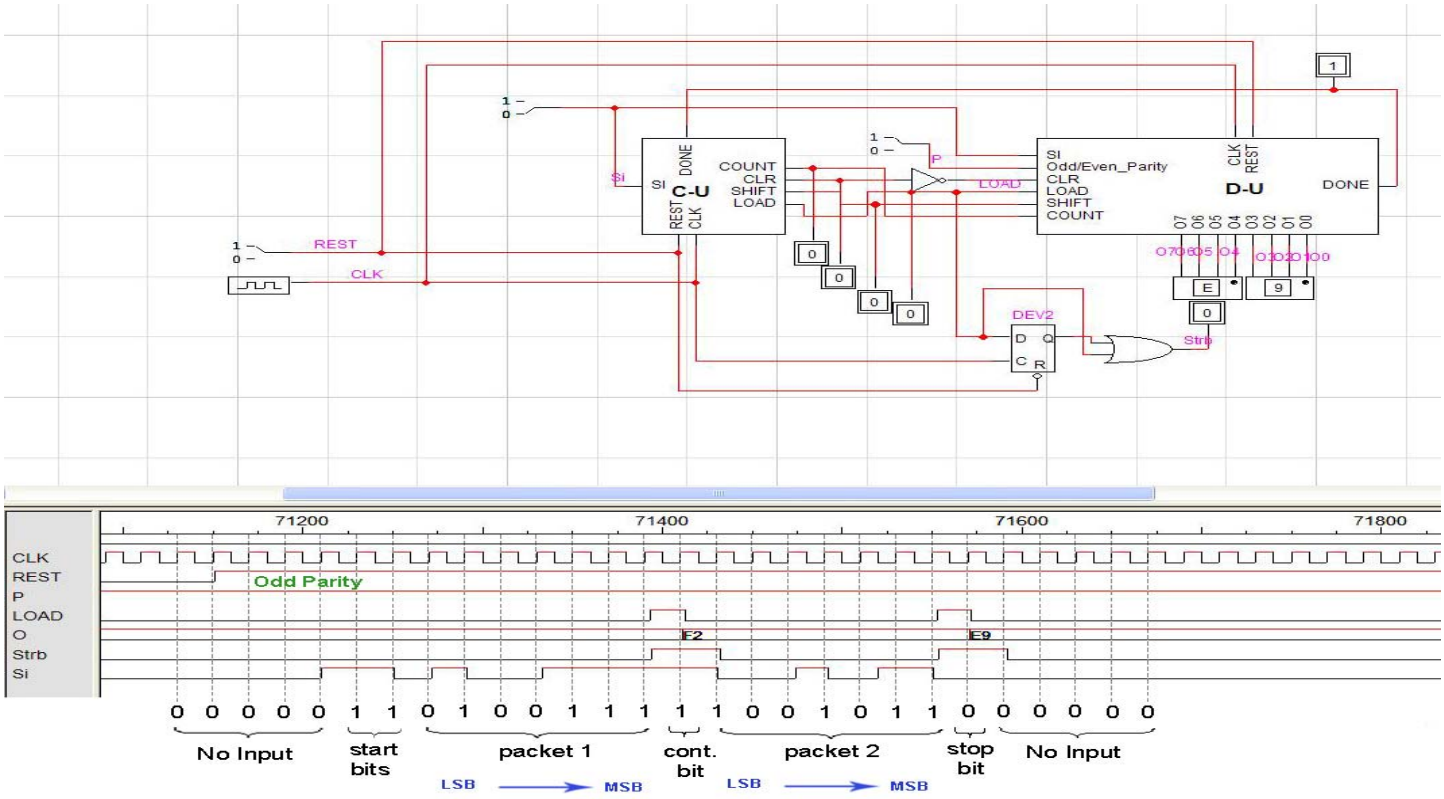


- **Even Parity test:**

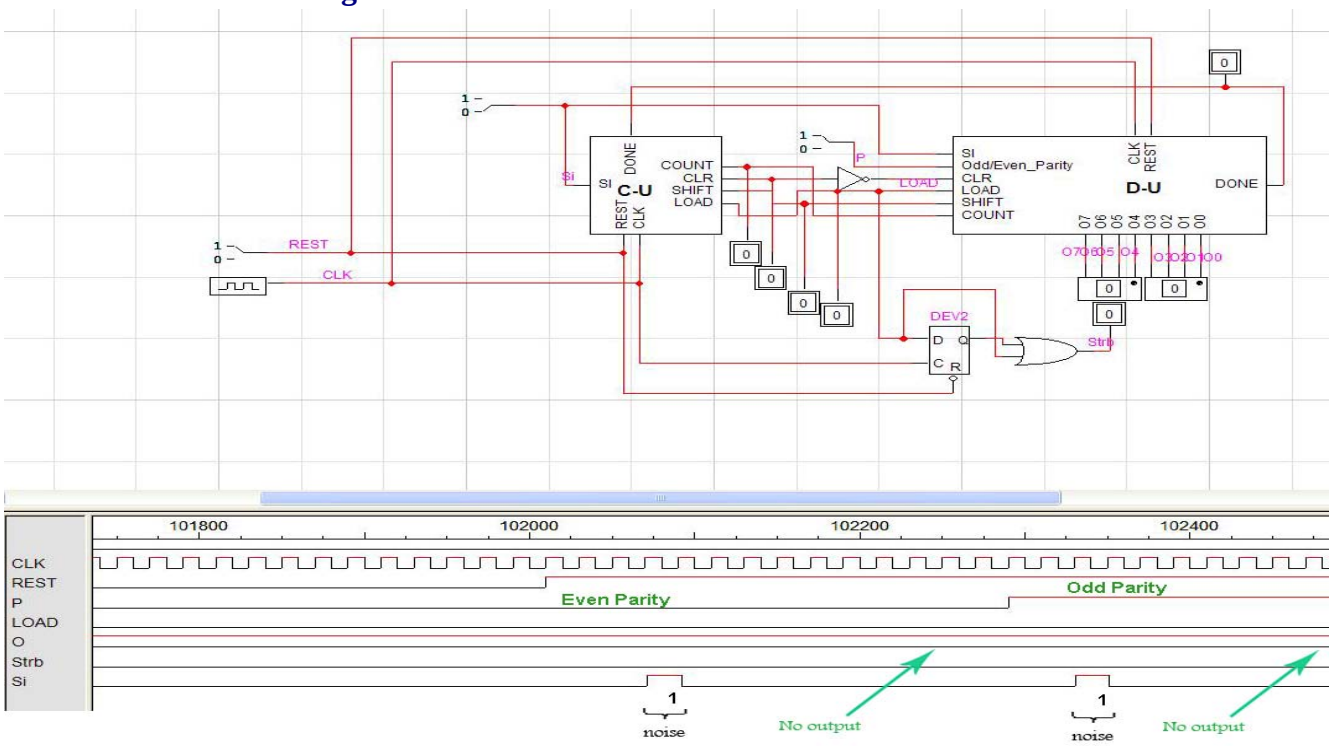




- **Odd Parity test:**



- **Noise Testing:**



CHAPTER V

CONCLUTION

Problems Faced:

1. How to find the library icon and we solve it by updating the LogicWorks through this link: http://www.capilano.com/downloads/logicworks/LW410Update.exe
2. How to create device symbols and we solve that by searching and we found this site: http://wadanet.com/hasegawa/book212/tool001.htm
3. After testing the circuit, a small glitch is found and we solve it by changing the state diagram.
4. After testing the circuit, we faced a big problem which is ignoring one bit after receiving the packet and we solve it by changing the state diagram.

Conclusion:

After finishing of phase I of the project, we learned many things. First of all, we improve our skills in designing digital circuits. Also, we learned how to use LogicWorks application to design and simulate circuits. Finally, we learned how to work as a team.