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A portable high-frequency digitally controlled oscillator (DCO)

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ABSTRACT

A novel digitally-controlled oscillator (DCO) is reported. Utilizing a new capacitive load, the new DCO is capable of producing much higher output frequencies than existing DCOs. All other components are fully digital and modular, allowing portability to any CMOS process and customization for different applications. At the heart of the DCO is a digital ring oscillator (DRO) that utilizes the new shunt-capacitive loads. Unprecedented higher frequencies are obtained through a novel idea of electrically removing the effect of un-enabled loads. Simple design conditions for achieving proper operation of the DRO are provided and verified through simulations with several technologies. Spice simulations verified the correct and superior operation of the DCO even with device mismatch. A custom layout of the DRO was generated using LFoundry's 150 nm technology. The total DRO area was found to be 418 μm^2. Comparison with other DCOs and VCO shows that the new DCO outperforms conventional DCOs in all aspects; maximum attainable frequency, power efficiency and required number of control bits to achieve a certain resolution.

1. Introduction

Many applications require the generation of high speed on-chip clocks with minimal area and power consumption. Analog Phase-locked loops (PLLs) can provide precise frequencies but contains analog circuits and filters that take up large chip area and cannot be ported from one fabrication process to another. All-digital PLLs are more portable and have considerably smaller areas. They, however, require digital DCOs with monotonic behavior, wide frequency range, fine frequency resolution and good period linearity.

Over the years, many DCOs have been proposed. Almost all of the reported DCOs use two stages for frequency tuning; a coarse tuning stage and a fine tuning stage. This allows the DCO to have a large frequency range with fine resolution while using a minimal number of control bits. This however, may also limit the maximum output frequency of the DCO. Most of the conventional DCOs employ one or more of the following techniques (Fig. 1) to change the delay:

(1) *Current-starved* inverters as delay stages [1–3,9,12,15], Fig. 1(a). Binary-weighted PMOS/NMOS transistors connected in series with the inverter's original PMOS/NMOS transistors are used to control the equivalent charging/discharging resistance of the inverter. This in turn, increases or decreases the inverter's delay. Maximum frequency is obtained when all the delay-controlling transistors are on. Resolution can be increased by increasing the number of binary-weighted load transistors. These transistors, however, significantly increase the inverter's intrinsic delay due to increased parasitic capacitance on internal nodes, increased charging/discharging paths, and most importantly due to the introduced body effect. All this limits the maximum attainable frequency and puts at odd with the resolution (which requires more load transistors). Some implementations use only NMOS transistors in the discharge path as not to weaken further the already weak PMOS transistors. Also, some researchers use MOS varactors with differential drive as shunt capacitors due to their excellent linearity [12–14]. This however requires a large number of delay stages due to the small capacitance of varactors.

(2) CMOS inverters *with switched shunt MOS capacitors* [4,5,12,13], Fig. 1(b). The MOS capacitors are also binary-weighted and are used to control the delay of the inverter by varying its capacitive load. Some implementations use complete transmission gates in place of the NMOS switches shown in Fig. 1 (b). This, however, increases the parasitic capacitance at the inverter's output node which represents the minimum possible load (i.e. determines the maximum frequency). Hence, increasing resolution through adding more switched capacitors reduces the maximum DCO frequency.

(3) *Path selection multiplexors* to select the number of delay stages in the DCO [1,6–11], Fig. 1(c). Path selection is seldom used on its own due to its limited resolution and is usually combined with other techniques (e.g. [1,9]).

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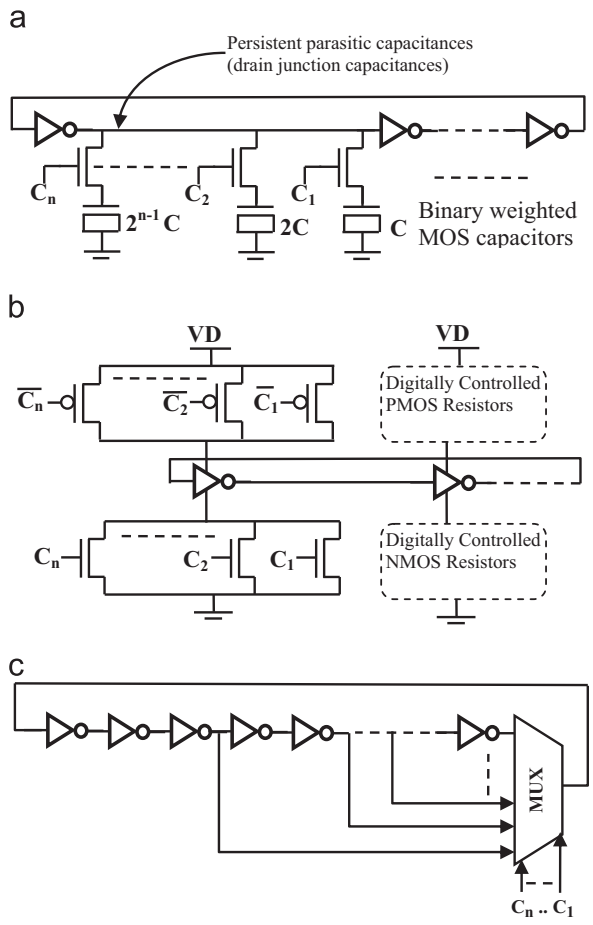

Fig. 1. Conventional techniques for implementing DCOs. (a) A digital oscillator based on shunt MOS capacitors, (b) a digital oscillator based on current starving, and (c) a digital oscillator based on path selection.

Although all the above mentioned techniques were effectively used to produce fine resolution and large frequency range with adequate linearity, they all suffer from a basic shortcoming; limited achievable maximum frequency. This is due to the fact that whatever technique is used to control the DCO's period, the elements that are used to control the delay (series resistances, shunt capacitors, or selection multiplexors) always exist in the circuit and cannot be physically eliminated at the highest DCO frequency. Also, switches (NMOS, PMOS or transmission gates) controlling these elements introduce significant parasitic capacitances reducing the DCO's maximum attainable frequency further. These two issues lead to a basic trade-off in all existing DCOs; in order to increase the resolution and/or frequency range, more delay elements have to be added which reduces the DCO's intrinsic (maximum) frequency. Also, in order to increase the range, the range of values of the binary-weighted resistors or capacitors (used as delay control elements in the DCO) must be increased. This reduces the inverters' output signals slope which in turn reduces the DCO's period linearity with the control word. It also causes matching problems and can lead to non-monotonic DCO frequency characteristics at some control code words (non-uniform frequency change between adjacent code words). This also forces designers to use the highly non-linear MOS capacitors to be able to get large capacitance values with reasonable silicon area.

The developed DCO circuit solves the above mentioned problems to a large extent by electrically removing delay elements (shunt capacitors) that are not enabled by the digital control word. This allows obtaining a maximum intrinsic frequency (when the control word is all 0 s) close to that of an unloaded oscillator. It also allows obtaining the desired frequency range with much smaller values of shunt capacitors. In Section 2 the general architecture of the proposed DCO is introduced followed by a detailed description of the digital ring oscillator (DRO) which is the core of the DCO in Section 3. Simulation results showing the superior operation of the operation of the DRO are shown in Section 4. A custom layout of the new DRO is presented in Section 5 to illustrate the small area of the new DRO. Finally, conclusions are presented in Section 6.

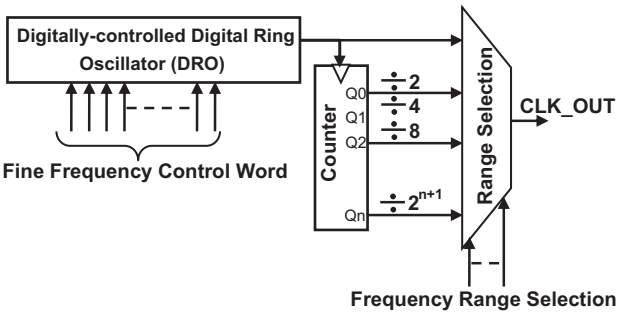

Fig. 2. The architecture of the newly proposed DCO.

2. The proposed DCO architecture

Fig. 2 below shows the general architecture of the proposed DCO. It is made of a novel digitally-controlled digital ring oscillator (DRO), a frequency divider (binary counter) and a range selection multiplexor (MUX). The DRO generates the basic (or intrinsic) high frequency range that is equal to at least one octave, i.e. $f_{min} \leq 0.5 f_{max}$ (where f_{max} is the DRO's maximum frequency and f_{min} is the minimum DRO frequency). Then through division by powers of 2, the counter generates the lower frequency ranges and the MUX provides the range selection. The DRO's basic range of at least one octave ensures continuous frequency range with the successive division by 2. As such, the required range of the DRO is relatively small, allowing for finer resolution with fewer control bits. It also means that the maximum shunt capacitance is significantly reduced, preserving the DRO's output signals' slopes and improving linearity. The reduced range of capacitance values also makes it easier to ensure monotonicity of the oscillator with process variations.

It should be noted that due to the DRO's f_{min} being set to slightly less than $0.5 f_{max}$, there will be a small overlap between adjacent frequency sub-ranges (i.e. different codes giving the same frequencies). Unlike non-monotonic behavior, this overlap will not cause any stability problems in PLLs or DDLs utilizing this DCO since these overlap regions do not have adjacent codes.

3. The digital ring oscillator (DRO)

3.1. DRO circuitry

As Fig. 3(a) shows, the DRO is made of an even number of Digital Delay Stages (DDS) and a special gate, the merging NAND (MNAND) gate. The MNAND structure, Fig. 3(b), was developed to achieve higher DRO frequency, but could be replaced by regular CMOS gates for standard cell-based design as shown in Fig. 3(b). Each DDS has two identical CMOS inverters with a novel capacitive load cell connected between their outputs, Fig. 3(c). The DDSs and the MNAND form two digital ring oscillators with identical inverters that oscillate at the same frequency and phase.

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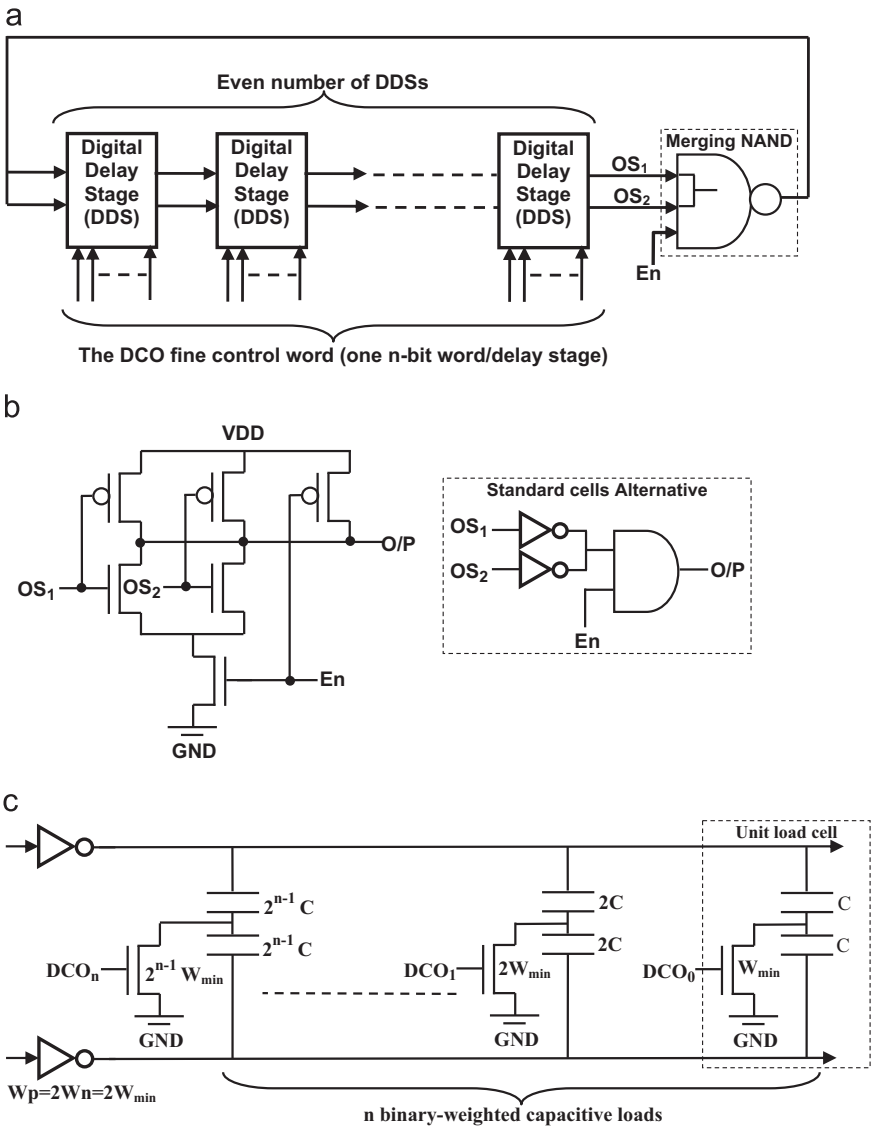

Fig. 3. The digitally-controlled digital ring oscillator (DRO). (a) Basic structure of the DRO, (b) the merging NAND gate, and (c) a Digital Delay Stage (DDS)

The newly developed, binary weighted, digitally controlled, capacitive loads are connected between each delay stage in one oscillator and the corresponding stage in the other oscillator. Each capacitive load cell is made of two identical capacitors connected in series with an NMOS switch that conditionally connects the node in between them to ground. These switches are controlled by the DCO's fine frequency control word. The MNAND gate is used to reset the oscillators to start at the same exact moment and 'merges' the two oscillators' last-stage signals ensuring phase and frequency synchronization between the two oscillators under process and voltage variations. It produces a constant high output when the En (enable) input is low. When the En input is high, it acts as a wired-gate (made of two inverters with their outputs tied together) that 'merges' the two inputs into a single output that is the time interpolation of the two inputs.

3.2. Concept of operation

As was shown in Fig. 1(a), conventional shunt-capacitor DCOs place the capacitor after the switch. This enables the use of MOS capacitors as loads. Fig. 4 illustrates the basic concept of the new capacitive load. By simply exchanging the positions of the switch and load capacitance (Fig. 4(a) and (b)) the off capacitance is reduced by $C/(C+C_j)$, where C is the unit capacitance and C_j is drain junction capacitance. The load capacitance now has to be a metal capacitor for isolation. This increases the maximum frequency by a factor of *up to* 2. Now if the drive is doubled by using two synchronized inverters with identical loads and a single switch, as in Fig. 4(c), the maximum frequency is further increased by another factor of *up to* 2. This is because the capacitor combination is driven from both ends with identical phase hence the two inverters in the two oscillators see very small capacitances ($<0.5C_j$). When the switch is on, the common node is connected to ground and each inverter sees a load of C which increases its delay while identical phase is still maintained, Fig. 4(d). Hence, unlike conventional shunt capacitance schemes, this new scheme results in a large capacitance difference between the two states. The increase in maximum frequency is usually limited to about $2.5\times$ of conventional DCOs due to the inverters' own output parasitic capacitances.

The large difference between the ON and OFF capacitances means that the required frequency range and resolution could be obtained with small values of C and few load cells. It should be noted here that the shunt capacitances must be implemented with metal layers not MOS capacitors to avoid excessive parasitic capacitances. This however is not a problem since the required

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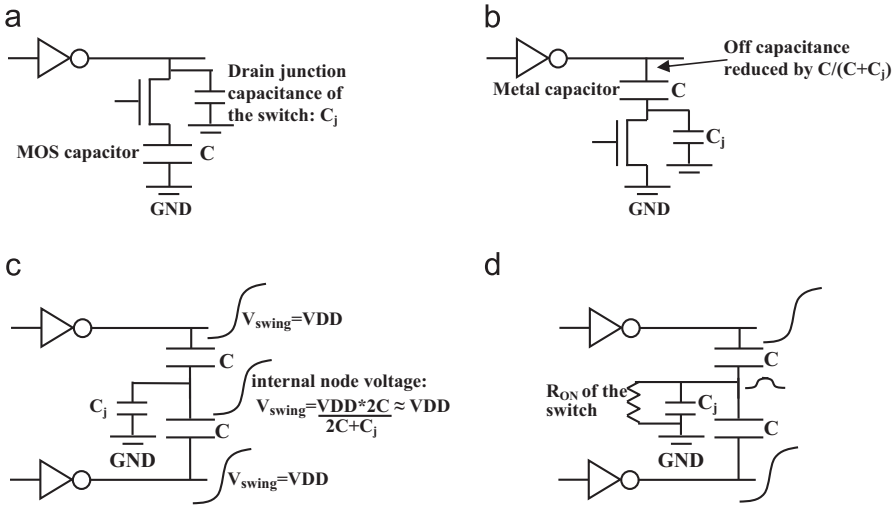

Fig. 4. Concept of operation of the new capacitive load cell. (a) Conventional shunt-capacitive load: Even when the switch is off the inverter sees a load, (b) exchanging the capacitive load with the switch, when switch is off the inverter sees a load $< C_j$, (c) with double drive: when the switch is off, each inverter sees a load $=0.5(CC_j)/(C+0.5C_j)$ $<0.5C_j$ and (d) when the switch is ON, each inverter sees a load $\approx C$

values are very small. For example, for a 3-stage DRO implemented in a 0.13 μm technology with 4-bit/stage control, the required value of C is 0.5 fF. This yields an astonishing DRO frequency range of 2.5–5 GHZ. The on-chip area of such a capacitor would be in the order of few square micrometers.

3.3. Design constraints

For proper portability of the DRO to any fabrication process, it has to be ensured that $f_{max} \geq 2f_{min}$. This means the maximum delay through a DRO stage must be at least twice its minimum delay, i.e. $T_{Dmax} \geq 2T_{Dmin}$. Also, to improve linearity of the DRO, the sizes of the NMOS switches in the capacitance cells have to be increased at the same ratio of the capacitance (i.e. binary-weighted fashion).

Now the minimum value of C (the unit load capacitance, Fig. 2 (c)) that is needed for proper DRO operation can be estimated as follows; first, the following two equations give approximate values of T_{Dmax} and $2T_{Dmin}$ for a 3-stage DRO based on simple RC delay model:

$$T_{Dmin} = R_{eq}[2C_{in} + 0.5(2^n - 1)C_j] \quad (1)$$

$$T_{Dmax} = R_{eq}[2C_{in} + (2^n - 1)C] \quad (2)$$

Where R_{eq} is the equivalent resistance of the CMOS inverter in the DDS, C_{in} is its input capacitance, C_j is the unit drain junction capacitance of the NMOS switch in the capacitance cell (its value is split between the two inverters), and n is the number of control bits/DDS. In (1) and (2) above, the delay of the MNAND gate (which is relatively constant) is divided among the two DDSs, hence the factor of 2 in front of C_{in}. The intrinsic delay of the MNAND is approximately twice that of the inverters in the DDSs since it has twice the FanOut. So from the above equations, the condition for proper operation of the DRO was obtained a

$$C \geq \frac{2C_{in} + (2^n - 1)C_j}{(2^n - 1)} = \frac{2C_{in}}{2^n - 1} + C_j \quad (3)$$

For example for a 0.13 μm, 1.2 V technology, the values of C_{in} and C_j were 1.6 fF and 0.27 fF, respectively. According to the condition obtained above and for 4-bit control/DDS, the value of C should be 0.48 fF. The actual value found from simulations was actually 0.50 fF, showing excellent agreement with the predicted value. Table 1 below shows the predicted (using Eq. (3)) value of C for several process technologies and the actual value obtained from simulations by tweaking C till the condition $f_{max} \geq 2f_{min}$ is achieved. It also shows the achieved maximum frequency at each node. These results show excellent agreement between predicted and actual values of C. This means designers could use Eq. (3) above to estimate C, simulate the circuit with this value and then do little 'tweaking' to get the right condition for proper operation of the DCO operation (i.e. $f_{max} \geq 2f_{min}$). This eases portability to any process. It should be noted here that for all these technologies, minimum-sized inverter cells were used in the DRO with unprecedented obtained frequencies.

Table 1
Calculated versus actual values of C (obtained from spice simulations) for several process technologies.

Process	180 nm	130 nm	90 nm	65 nm
Supply voltage	1.8 V	1.2 V	1.2 V	1.2 V
C_{in}	1.550 fF	1.60 fF	0.289 fF	0.221 fF
C_j	0.474 fF	0.27 fF	0.091 fF	0.092 fF
Calculated value of C	0.680 fF	0.48 fF	0.13 fF	0.121 fF
Actual value of C	0.643 fF	0.50 fF	0.15 fF	0.118 fF
F_{MAX} (GHz)	4.42	5.08	7.76	8.41

3.4. DRO control schemes

Since each DDS has its own control word, there are many ways to control the DRO. All words cannot be concatenated together as one big binary-coded word because that will result in many redundant codes (producing equal frequencies) which in turn will cause non-monotonic RDO characteristics. As such, there are two main ways to properly control the DRO to ensure non-redundant codes; one way is to control the DDSs in a round-robin binary fashion and the other is to control all the DDSs' loads together in a thermometer coding fashion. In the first method, starting with the first DDS, its control word is incremented till it reaches its maximum value, then the control word for the 2nd DDS is incremented till it reaches its maximum value, then the control word for the 3rd DDS is incremented and so on, Fig. 5(a). This is equivalent to dividing the frequency range into a number of sub-ranges equal to the number of DDSs.

In the second DRO control method, Fig. 5(b), the load capacitances are enabled in a thermometer coding fashion; 1st C (the smallest capacitance) of the 1st DDS is enabled, then that of the

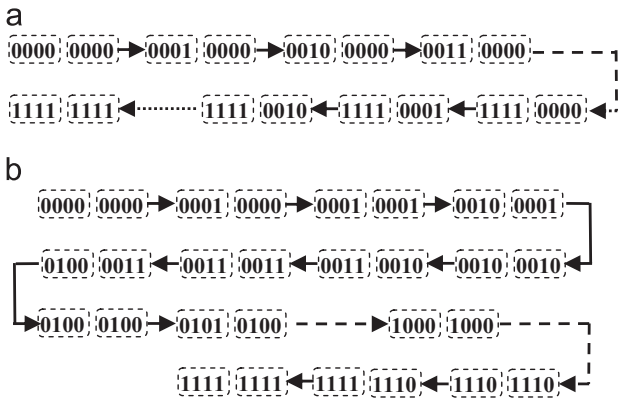

Fig. 5. The two main methods for controlling the DRO (illustrated for 2 DDSs with 4-bit/stage control words). (a) Controlling the DDSs in a binary round-robin fashion and (b) controlling the DDSs in a thermometer coding fashion.

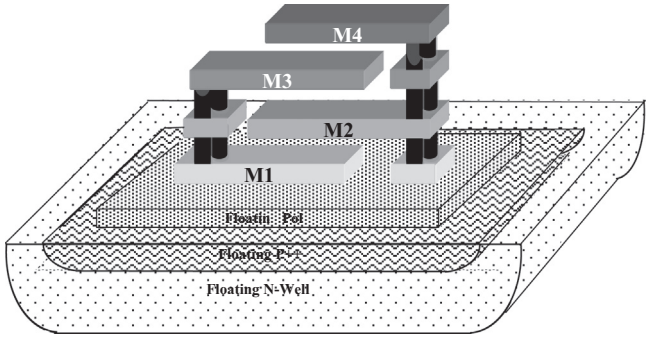

Fig. 6. A 3-D layout of a 4-layers metal capacitor. The dimensions of the floating layers (Poly, P++ and N-well) have been exaggerated for clarity.

2nd DDS, then that of the 3rd DDS till the last DDS's *C* is enabled. Next 2*C* of the 1st DDS is enabled and its *C* is disabled, then the 2*C* of the 2nd DDS is enabled and its *C* is disabled, and so on till all the 2*C*s are enabled. Then another round of enabling the *C*s, followed by a round of enabling the 4*C*s and disabling *C* and 2*C* of each DDS. This will be followed by another round of enabling the *C*s, and then the 2*C*s, followed by a round of enabling the 8*C*s and disabling the *C*, 2*C* and 4*C* of each DDS and so on till all loads in all DDSs are enabled (minimum frequency). This method of control achieves better linearity but is slightly more complex to implement.

3.5. DRO's metal capacitances

As was explained before, the capacitors used in the DDS for delay control must be metal capacitors for isolation and low parasitic capacitance to ground (GND). If the used technology has a MIM (metal–insulator–metal) capacitor then this would be the best option as it provides the highest capacitance per unit area. MIMs are usually implemented with a high level metal and a special intermediate metal layer with a dielectric with a reduced thickness in between. Also, floating layers of lower metals are used to reduce the parasitic capacitance of the lower plate to GND (substrate). If the technology does not have a MIM, then multi-layered metal capacitors can be used as shown in Fig. 6. With at least 4 levels of metal and the use of floating layers as shown in Fig. 6, the parasitic capacitance could be kept under 10% of the capacitance. In all cases, the bottom plate of the capacitor should be connected to the NMOS switch in the delay cell.

4. Simulation results

4.1. Validation of the basic operation

To verify the validity of the new DCO design a 3-stage DRO (two DDSs) and a 3-bit counter were simulated with Spice using a 0.13 μm, 1.2 V CMOS technology. All NMOS transistor widths were set to a minimum of 1.5*L* (*L* is the minimum channel length) and that of the PMOS transistors to twice that (i.e. 3*L*). *C* was selected to achieve the required frequency criterion $f_{max} \geq 2f_{min}$, as explained before. Fig. 7 shows the voltage waveforms at the outputs of the first stage of both oscillators of the DRO (VOUT1 and VOUT2), and the internal node of the unit capacitance load cell (the smallest capacitance) for two conditions; (a) when all control words are 0 s (maximum frequency), and (b) when the 1st control word is 0011 (three steps above minimum period). The corresponding oscillation periods (*T*) are also shown on the figure. This figure illustrates how the concept of the new capacitive load cell works; when the switch is OFF, the internal node follows the inverters' outputs very closely, resulting in very small 'effective' capacitive loads for these inverters, thus the attained extremely high frequency. Also, the two oscillators remain in-phase all the time (with or without the capacitive cells enabled).

Fig. 8 shows the period and frequency of the DRO's output with the two types of control methods. As this figure shows, the thermometer coding method produces a very linear response. It

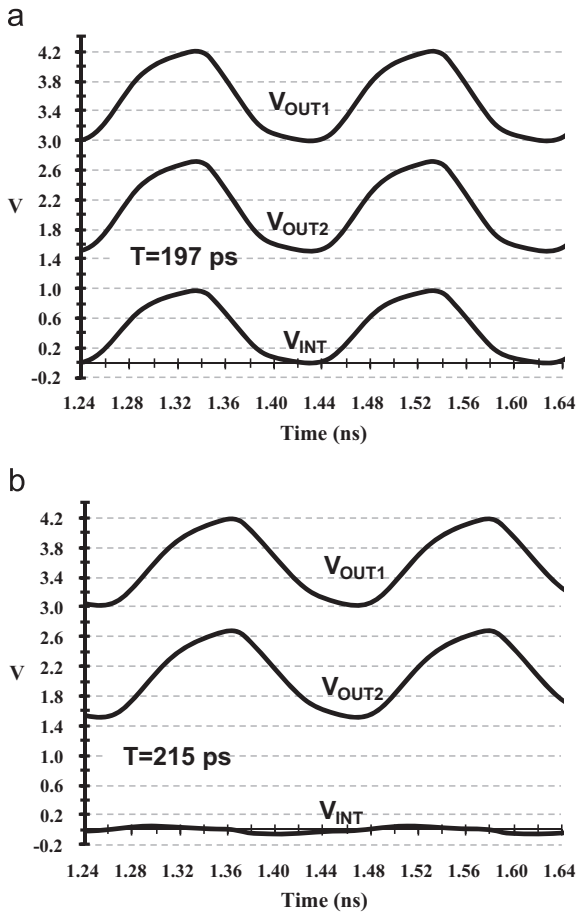

Fig. 7. The voltage waveforms of the 1st stage of the DRO and internal node of the unit capacitance load cell. (a) Voltage waveforms with the NMOS switch in the capacitance cell off; the internal voltage tracks the inverters' output hence the inverters practically see no capacitance and maximum frequency is obtained (*T* is the period). V_{out1} and V_{out2} have been shifted up for clarity and (b) the waveforms with the NMOS Switch ON; the internal voltage is held close to 0 V (i.e. the inverters in the DRO see the full load capacitance.

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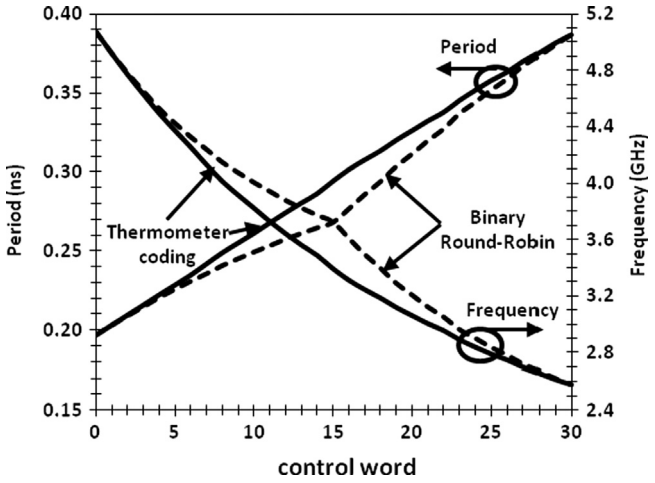

Fig. 8. The DRO's characteristics (period/frequency versus control word) using the two control methods.

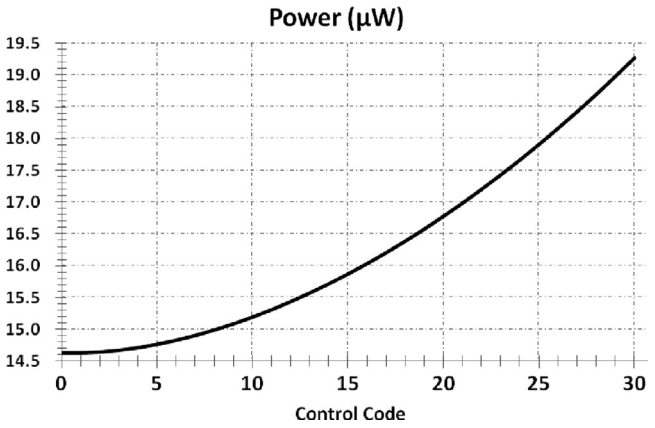

Fig. 9. Power consumption of the DRO; power increases as frequency decreases.

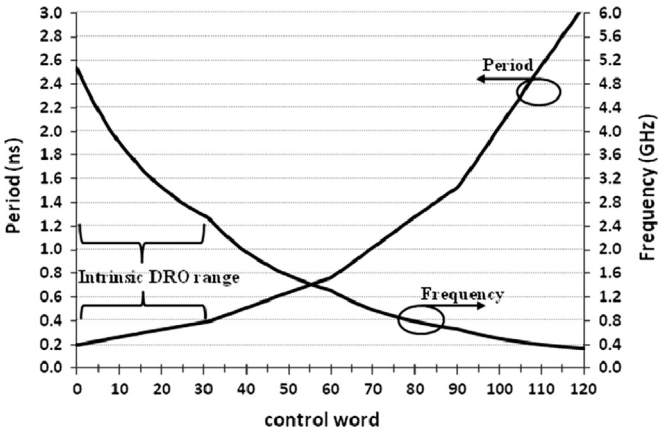

Fig. 10. DCO's frequency characteristics. Code words 0–30 represent the basic DRO range. Other ranges are obtained through division with a 3-bit counter.

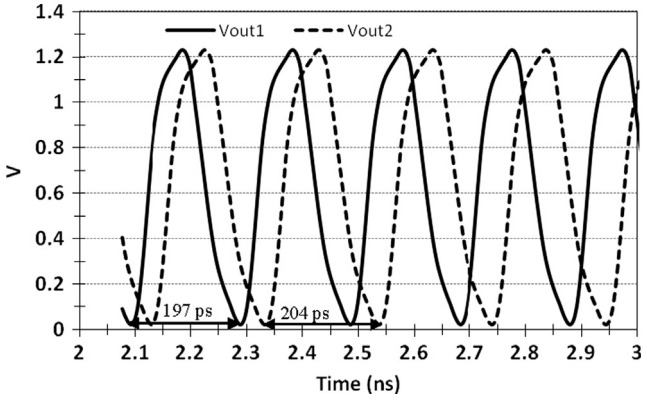

Fig. 11. The DRO's output waveforms with and without device mismatch between the two oscillators.

also shows that with only 4-bits of control word/stage the period step is ~6 ps, a remarkable performance. Lower frequency ranges, obtained through frequency division, will have larger period steps. Also, when using the binary round-robin control, the period step slightly increases as we move from the 1st DDS to the second DDS due to the effects of increased signal slopes. Hence there will be a set of sub-ranges within the DRO's intrinsic range equal to the number of DDSs within the DRO when using this type of control. The DRO's response is still very acceptable.

Fig. 9 shows the power consumption of the DRO versus the control word. At lower frequencies (higher codes) the power actually increases even though the frequency decreases. This is because lower frequencies are obtained by increasing the capacitive loads at the outputs of the oscillators' inverters. This not only compensates for the decrease in frequency, but also reduces the slope of signals which in turn increases the short circuit currents in the inverters.

Fig. 10 shows the DCO's frequency/period characteristics with the three sub-ranges. It should be noted that, when lower frequency ranges are obtained through successive divisions by 2, non-montonic transitions at the borders between adjacent ranges may occur due to f_{max} being $> 2f_{min}$. This, however, will not cause any problems since the transition from one range to another is accomplished using the selection MUX while the DRO has the same frequency (i.e. the DCO would go from a frequency f to 0.5f, 2f, 0.25f, or 4f…etc.). So any search algorithm used in a feedback loop (such as in a digital PLL) will not be stuck in a non-monotonic region.

4.2. *Effects of devices mismatch*

As explained above, the new DCO utilizes two oscillators that must oscillate in perfect synch for the new load cell to operate properly. One concern might arise; what would be the effect of devices mismatch between the two oscillators? The concern here is that the device mismatch would cause phase mismatch between the two oscillators. With such phase mismatch, capacitances in cells that are off which are suppose to 'appear' as open circuited would have an actual value that depends on the mismatch. To check this concern the DRO was simulated with the channel lengths of all MOS transistors in one of oscillator being 10% larger than the minimum. This goes beyond any reasonable process mismatch. Fig. 11 shows the output of the DRO at maximum frequency (the most sensitive point to phase mismatch) without the mismatch (V_{out1}) and with the mismatch (V_{out2}). As this figure clearly shows, the capacitive cells (and the DRO) still operate exactly as they should. The MNAND gate actually 'mixes' the two oscillators frequency and the resulting frequency is an interpolation between the two. The 10% increase in the channel length of one of the oscillators increased its period by ~7%. The net result, as shown in Fig. 11, is that the DRO's period actually increased by ~3.5%.

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4.3. Performance comparison

The performance of the proposed DCO was compared to a conventional 3-stage, 4-control bits/stage, shunt-capacitive-load DCO. Fig. 12 shows the period and frequency of both DCOs versus the control word. For fair comparison, both DCO's had the same inverters' sizes but the loads were adjusted such that the ratio between $f_{max}/f_{min} \sim 2$. As this figure shows, the new DCO can achieve double the maximum frequency of the conventional DCO due to the new capacitive cell. It also has a much better linearity than the conventional DCO.

Table 2 shows a comparison between the new DCO and several published DCOs in terms of number of control bits, maximum frequency, power efficiency and resolution. For completion, a recently used [16] current-mode analog VCO (voltage-controlled-oscillator) was also included in the comparison. Power efficiency was calculated by dividing the reported power by the frequency and by the square of the voltage supply. This normalizes the power across different manufacturing processes and supplies. As Table 2 shows, the new DCO outperforms all other DCOs and VCO in terms of the required number of control bits, power efficiency and maximum frequency. One notable achievement of the new DCO is that its maximum frequency at the 0.18 μm technology node (4.42 GHz) exceeded that of the analog current-mode VCO, something that was never achieved by digitally-controlled oscillator before. This is due to resolving the tradeoff between the required resolution and the attainable maximum frequency. This also has led to an enormous enhancement in the power efficiency. In fact, as was shown in Fig. 9, the power efficiency of the new DCO increases at higher frequencies, something that could not be achieved by any of the other DCOs.

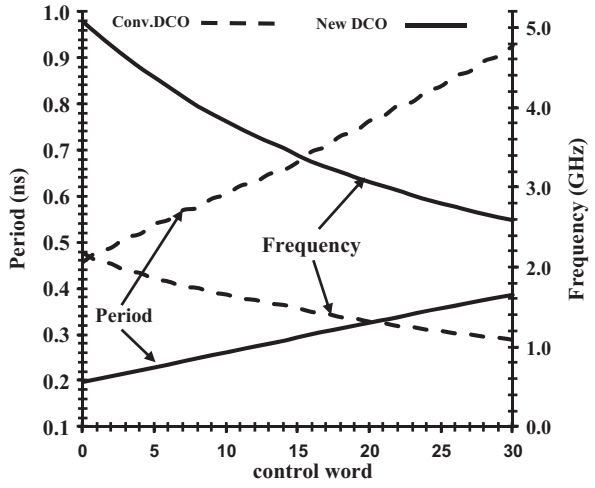

Fig. 12. Comparison results for the new DCO and a conventional DCO based on MOS shunt capacitive loads.

5. DRO area

A custom layout of the 3-stage, 4-bit control/stage DRO was generated using LFoundry's 150 nm technology and is shown in Fig. 13 below. M1–M4 capacitances were used for the load cells (at the top part of the layout) which were kept symmetrical and adjacent for matching. Also, the inverters in the DDSs were kept adjacent for matching. The MANAND was placed in the middle of the layout to reduce the interconnect length. The total DRO's area came out to be 44 μm × 9.5 μm (i.e. 418 μm^2), a remarkably small area even at this technology node.

6. Conclusions

A new fully-digital DCO has been developed. It utilizes a new type of shunt capacitive load for delay control. The new load significantly reduces the effects of parasitic capacitance resulting in a large increase of the maximum achievable frequency. Two methods for controlling the DCO have been devised. Also a simple yet very accurate equation was obtained for selecting the value of the unit capacitance load to ensure proper operation of the DCO. Simulation results with many technologies verified the accuracy of the obtained equation. These simulations showed that the proposed DCO achieved maximum frequencies ranging from 4.4 GHz at the 180 nm technology node to 8.4 GHz at the 65 nm technology node, an un-precedent performance. Simulations also showed that the new DCO is resilient to device mismatch. Comparison results showed the superior performance of the new DCO compared to conventional shunt capacitive load based DCOs. Also, the custom layout of the DRO shows its remarkable small area. Comparison with other published DCOs show that the new DCO significantly outperforms other DCOs in maximum frequency and power efficiency at the same resolution. Furthermore, it requires much less number of control-bits. The maximum frequency of the new DCO even exceeded that of an analog current-mode VCO, an unprecedented achievement by a DCO.

Table 2
Performance comparisons with other DCOs.

DCO	Control word length	Max. freq.	Power efficiency[a]	Resolution (LSB)
[15] A pure current starved DCO using a **32 nm, 0.9 V** technology	12-bits	800 MHz	4.17 μW/MHz/V^2	1 ps
[8] Combining path selection with variable strength inverters (in a 90 nm, 1 V technology)	15-bits	952 MHz	0.7 μW/MHz/V^2	1.47 ps
[9] Combining path selection with Varactor-based fine-tuning delay cell (in a 90 nm, 1 V technology)	26-bits	163 MHz	1.02 μW/MHz/V^2	2 ps
[12] Combining path selection with varactor-based fine-tuning delay cell (in a 0.18 μm, 1.8 V technology)	13-bits	450 MHz	4.17 μW/MHz/V^2	2 ps
[13] Differential DCO combining current starvation with varactor loads (in a 0.13 μm, 1.2 V technology)	15-bits	2.1 GHz	0.67 μW/MHz/V^2	1 ps
[16] A differential current-mode VCO (in a 0.18 μm, 1.8 V technology)	N/A	2.48 GHz	Not available	2.4 ps/mV[b]
This work (The DRO in a 0.13 μm, 1.2 V technology)	8-bits effective[c]	5.08 GHz	5.2 nW/MHz/V^2	0.78 ps

[a] Normalized to 1 V supply by dividing by VDD^2.
[b] Equivalent to 11-bits digital control.
[c] Translated to 7-bits per delay stage.

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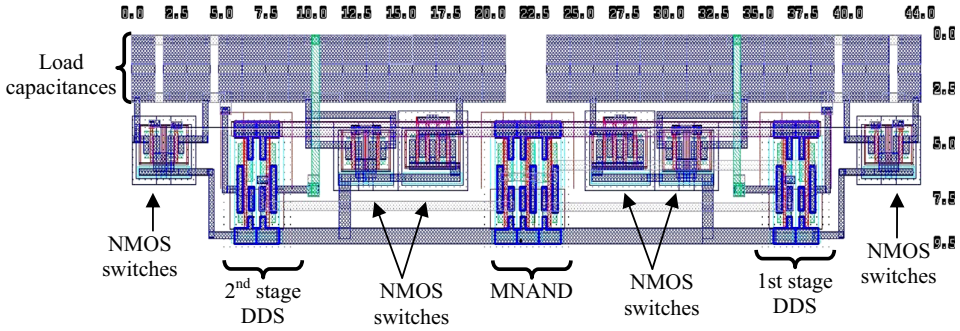

Fig. 13. Custom layout of the DRO using LFoundry's 150 nm technology.

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