Low-Power BiCMOS Circuits for High-Speed Interchip Communication

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Abstract—A universal BiCMOS low-voltage-swing transceiver (driver/receiver) with low on-chip power consumption is reported. Using a 3.3 V supply, the novel transceiver can drive/receive signals from several low-voltage-swing transceivers with termination voltages ranging from 5 V down to 2 V and frequencies well above 1 GHz. Measured results of test circuits fabricated in 0.8-µm BiCMOS technology are also presented.

Index Terms—BiCMOS integrated circuits, buffers, circuit simulation, current-mode logic, digital integrated circuits, feedback circuits.

I. INTRODUCTION

BiCMOS technology has proven to be an excellent workhorse for telecommunication applications [1]. These applications increasingly require higher circuit speeds and higher chip-to-chip bit rates. Also, for ever increasing complexity of telecommunication switches, the need arises for transceivers (driver/receiver) with low on-chip power consumption that can operate at low supply voltages.

Bipolar circuits such as emitter coupled logic (ECL) or current mode logic (CML) can meet the speed requirements at the expense of large power consumption. Different dynamic circuit techniques that reduce the power consumption of ECL/CML logic circuits while maintaining or increasing their speed were recently reported [3]–[6]. However, these techniques were intended for bipolar VLSI logic applications and are not suited for ECL/CML output drivers’ applications that have higher current requirements. Recently, many low-voltage-swing driver circuits have been reported. These circuits range from reduced-swing CMOS [7] and CMOS pseudo ECL or CMOS 100 K ECL [8]–[9], to CMOS Gunning transceiver logic (GTL) [10]. The CMOS reduced-swing transceivers have limited speed, and the CMOS true or pseudo ECL are complicated to design and have high power consumption.

The GTL requires a special reference voltage. Also, each of these transceivers, as well as the true or pseudo bipolar ECL or CML transceivers, requires a different termination voltage, thus making them incompatible. Signal conversion parts, as well as multiple termination and reference voltages, would be required in systems using parts with different transceiver types, thus increasing the overall system cost and complexity.

In this paper a new universal low-voltage-swing low on-chip power BiCMOS transceiver is presented in Section II. Using a 3.3 V supply, this transceiver can operate with termination voltages ranging from 5 V down to 2 V. The performance of the different building blocks of the new transceiver is evaluated using both simulations and experimental results.

To realize these concepts, these circuits were fabricated in (0.8-µm, 5-V) BiCMOS technology [1], [2] of Northern Telecom with a bipolar junction transistor (BJT) $F_1$ of 12 GHz. These circuits were designed, simulated, and tested at 3.3-V power supply in 5-V technology.

II. THE LOW-VOLTAGE-SWING LOW-POWER UNIVERSAL TRANSCEIVER

The novel transceiver consists of a universal receiver and a universal output driver operating at a 3.3-V supply. The receiver can read signals with termination voltages ranging from 1.5 V to 5 V and the driver can drive an external 25 Ω terminated to a termination voltage $V_T$, ranging from 2 V to 5 V. Neither circuit requires the use of any external reference voltages. However, it is restricted to have level shifting of signals with respect to $V_T$ for this design. Hence, assuming the signal swing $V_s$ to be between 0.8 V to 1.0 V, all signals should be from $V_T$ to $V_T - V_s$.

A. The Universal Receiver

The receiver circuit consists of three subcircuits; the universal input buffer (Fig. 1), the $V_{ref}$ generator [Fig. 2(a)], and the load control circuit [Fig. 2(b)].

1) The Universal Input Buffer (UIB): The UIB is basically an emitter-coupled BJT pair followed by a source-follower stage. Four PMOS devices $M_{1-4}$ (Fig. 1) are used as loads for the emitter-coupled BJT’s. These load devices are controlled by the two biasing voltages, $V_1$ and $V_2$, which are generated by the load control circuit. The two PMOS devices, $M_5$ and $M_6$, ensure that the n-wells of all the PMOS devices $M_{1-6}$ are connected to the highest voltage among $V_T$ and $V_{DD}$. The value of the reference voltage $V_{ref}$ in Fig. 1 is kept at about $V_T - 0.45$ V by the $V_{ref}$ generator circuit.

For a termination voltage less than $V_{DD}$ (3.3 V), $M_1$ and $M_4$ will be off, and $M_2$ and $M_3$ will be on and act as loads for the differential pair. Hence, the output signal of the differential pair will be from $V_{DD}$ to $V_{DD} - V_s$. The n-wells of the PMOS devices $M_{1-6}$ will be connected to $V_{DD}$ via $M_5$. Similarly, when $V_T$ is greater than $V_{DD}$, $M_2$ and $M_3$ will be off, $M_1$ and $M_4$ will be on, and the differential pair output swing will be from $V_T$ to $V_T - V_s$. The PMOS n-wells will be connected to $V_T$ via $M_6$.
A source-follower stage was used instead of an emitter-follower one to avoid saturating the emitter-follower’s BJT’s when \( V_T \) is larger than \( V_{DD} \). This also ensures that the UIB differential output signal will not saturate the input devices of the driven gate. The speed is slightly reduced but the saturation problems are eliminated.

2) The \( V_{ref} \) Generator: \( V_{ref} \) is about 0.5 \( V_{BE} \) below \( V_T \) and is generated by the \( V_{BE} \) multiplier (made of \( Q_1, R \), and \( R/2 \)). \( M_{n1} \) is on only when \( V_T \leq 2.5 \) V and is used to compensate the decrease in \( Q_1 \) current. \( M_{p1} \) and the diode are used for temperature compensation. \( M_{p1} \) is biased in such a way that its drain current will increase linearly with \( V_T \). This will keep the current through \( Q_1 \) constant and hence \( V_{ref} \) will always remain constant with respect to \( V_T \). Also, as the temperature increases, the drain current of \( M_{p1} \) decreases, and hence, the emitter current of \( Q_1 \) will increase and compensate the decrease in \( V_{BE} \) that occurs as the temperature increases (which is about \(-2.5 \) mV/°C). The reverse happens when the temperature decreases.

Fig. 3 shows the measurement results for the output of the \( V_{ref} \) generator versus temperature for several termination voltages. This figure shows the stability of \( V_{ref} \) over a wide range of temperatures and termination voltages. The maximum change in \( V_{ref} \) over the whole temperature range for all values of termination voltages was about 51 mV (about 5% of the voltage swing).

The measurement results for \( V_T - V_{ref} \) versus \( V_T \) at room temperature (25°C) are shown in Fig. 4. Two sets of data were measured from two randomly selected, different dies that came from two different wafers that were fabricated in two separate runs. This figure shows the accuracy of the generated \( V_{ref} \) for various termination voltages and its insensitivity to process. The two data sets are very consistent, and for most values of \( V_T \), the maximum deviation of \( V_{ref} \) from the required value is less than 20 mV. The largest deviation in \( V_{ref} \) occurred at \( V_T \)'s between 2 V and 2.5 V, which is the transitional region between the two ranges of operation (above 2.5 V and below 2.5 V) where \( M_{N1} \) turns on. However, the deviation is still less than 50 mV and consistent between the two wafers.

3) The Load Control Circuit: This circuit is a simple source-coupled NMOS pair with cross-coupled PMOS loads. The input and load MOS devices are connected and sized in such a way that when \( V_T \) is less than \( V_{DD} \), \( V_1 \) will be “High” and close to \( V_{DD} \) (i.e., \( V_{DD} - V_1 \) would be less than the
PMOS threshold voltage $V_{TP}$, and $V_2$ will be “Low.” When $V_T$ is greater than $V_{DD}$, $V_2$ will be “High” and close to $V_T$ ($V_T < V_{TP}$), and $V_1$ will be “Low.” This ensures the correct operation of the UIB and that no current will be flowing between $V_T$ and $V_{DD}$ under any circumstances.

The outputs $V_1$ and $V_2$ versus $V_T$ are shown in Fig. 5. This figure shows the correct operation of the circuit. The load control circuit was found to be very stable over the temperature range. The maximum change in $V_1$ and $V_2$ over the temperature range for any value of $V_T$ was found to be less than 10 mV.

4) The Receiver Performance: The simulated eye-diagram of the UIB with a tail current of 1 mA at 1 GHz input frequency is shown in Fig. 6 for two values of $V_T$ (2 and 5 V) and an ECL gate as a fan out. This diagram was generated by applying random 7-b data streams to the UIB’s input and overlaying the output responses. As this figure shows, the UIB functions perfectly for the two termination voltages and the intersymbol interference is very minimal.

The measured differential output waveforms of an ECL driver being driven by the new receiver at a frequency of 1.5 GHz are shown in Fig. 7. The receiver’s input signal was terminated to 2 V and the UIB’s tail current was 1 mA. This shows that the receiver operated at this high frequency and correctly switched the ECL driver. The total power of the receiver was 12.5 mW. Measurements also verified the operation of the receiver for $V_T$ ranging from 1.5 V to 5 V at this frequency.

B. The Universal Output Driver (UOD)

Two versions of the universal output driver were developed, Fig. 8. For the design of both drivers, double termination (25 $\Omega$ load to $V_T$) was assumed.

The UOD utilizes a dynamically controlled biasing network to switch a current between two values; a high value when the output is being pulled down and a low value (zero for the UOD1) when the output is being pulled high. Thus, unlike conventional CML drivers, the tail current is turned off when it is not needed.

1) The UOD1: The UOD1 works as follows: The voltage $V_c$, which in conjunction with $R_s$ determines the value of the tail current, is equal to the difference between the voltages at
$V_a$ and $V_b$ as shown below

$$I_z = \frac{V_b}{R_z} = \frac{V_a - V_c}{R_z}. \quad (1)$$

Hence

$$V_c = V_a - V_b. \quad (2)$$

So when the input $I/P$ is “High” (i.e., $I/P = V_{DD} - V_{BE}$)

$$V_a = V_{DD} - 2 \cdot V_{BE}, \quad V_b = V_{DD} - (1 + z) V_{BE}. \quad (3)$$

Hence

$$V_{CHigh} = V_a - V_b = z \cdot V_{BE} \quad (4)$$

where $z$ is the multiplication factor of the $V_{BE}$ multiplier made of $Q_1$ and the two resistors $R$ and $zR$. $z$ was adjusted such that $V_{CHigh}$ is about 1.2–1.3 V (i.e., $z$ is from 1.5 to 1.8) and $R$ was adjusted such that the “High” value of the current is around 32 mA. Also, since $V_c$ (and hence the value of the generated tail current) depends on the difference $V_a - V_b$, the tail current value is independent on supply variations provided that both the predriver and the driver are using the same supply voltage. When $I/P$ is “Low”

$$V_a = V_{DD} - V_{BE} - V_s, \quad V_b = V_{DD} - (1 + z) V_{BE} \quad (5)$$

hence $V_c$ becomes

$$V_{CLow} = z \cdot V_{BE} - V_s \quad (6)$$

where $V_s$ is the input voltage swing. The capacitances $C_{x}$’s are used to enhance the speed and resolve (to some degree) the above tradeoff. Meanwhile, they do not affect the dc characteristics. The following condition is imposed on $z$ to ensure that the “Low” current is zero (when $I/P$ is low $V_c$ would be $\leq V_{BE}$):

$$1 < z \leq 1 + \frac{V_s}{V_{BE}}. \quad (7)$$

Hence, for this driver to be designed properly, a rough value of $V_s$ should be known in advance. The “High” value of the tail current, however, is still independent of the exact value of $V_s$ ($V_{CHigh} = z V_{BE}$).

This circuit has two shortcomings. 1) The large BJT $Q_3$ is turned on/off solely through the base. Hence, the base resistance $R_B$ makes the turn-on/off slower than a combined base/emitter turn-on/off (such as in CML/ECL circuits). 2) The “Low” value of the tail current might not be exactly zero although it is designed to be so (it may reach a few hundreds of $\mu$A’s) due to the tolerance in the resistors in the biasing network. This would slightly reduce the noise margins by reducing the value of $V_{off}$ (the output high value).

2) The UOD2: To overcome the two shortcomings of the UOD1 mentioned above, the UOD1 circuit was slightly modified to produce the second version of the universal output driver, UOD2 (Fig. 16). A BJT, $Q_4$ (much smaller than $Q_3$), is added with its base connected to a voltage reference, $V_T$, to steer the current when $V_c$ is “Low.” Hence, the restriction on $z$ is relaxed ($V_{CLow}$ can be $> V_{BE}$). This increases the speed by making the voltage swing of $V_c$ smaller. Also, when $I/P$ becomes high, the “Low” tail current is steered away from $Q_4$ to $Q_3$ and helps in turning $Q_3$ on faster. The “Low” value of the current is much smaller than the “High” value due to two reasons. 1) $V_T$ is set to a value less than the “High” value of $V_c$, and 2) since $V_{BE}$ of $Q_4$ is larger than that of $Q_3$ (due to the size difference), the voltage drop across $R_s$ is smaller when $I/P$ is low.

Fig. 9 shows the measured output waveforms of both drivers at 500 MHz and a termination voltage of 5 V. The on-chip power at that frequency were 75 mW and 80 mW for the UOD1 and the UOD2, respectively. The power of a CML driver at the same termination voltage would be about 125 mW. An ECL or pseudo ECL driver would have an even greater power at the same conditions. For a 2-V termination, the UOD1 and the UOD2 powers are 25 mW and 29 mW, respectively.

Fig. 10 shows the eye-diagram of the UOD2 at 1 GHz. This diagram was generated in a similar manner to that of Fig. 6. As this figure indicates, there is no significant intersymbol interference due to the current switching and the use of decoupling capacitances in these drivers.

Fig. 11 shows the $F_{max}$ of the two drivers (defined as the frequency of operation where the output of the driver drops to 70% of its low-frequency value). It shows superior speed performance of UOD2 over the $V_T$ range. It also shows that for both drivers $F_{max}$ decreases as $V_T$ decreases due to the increase of the collector capacitance and the saturation effects of $Q_3$. The decrease of UOD2’s speed with $V_T$ is faster. Other disadvantages of UOD2 compared to UOD1 are the
slight increase in power and area, and the need for an extra reference voltage.

Fig. 12 shows the measured output waveform of the UOD1 at 1 GHz and 5 V termination. This figure shows that the output voltage swing is still 0.8 V (the same as the low-frequency swing) at this high frequency. Table I summarizes the power performance of the new transceivers compared to the conventional CML interface for different conditions. This table shows the superior power performance of the new circuits.

III. CONCLUSION

Circuit techniques that take advantage of existing BiCMOS technologies and enhance interchip communication were developed. The novel transceiver operated with termination voltages ranging from 2 to 5 V, without the need for an off-chip reference voltage. The good performance of the biasing circuits was demonstrated over a wide range of temperatures and termination voltages. The new drivers would have lower on-chip power than ECL/CML or pseudo ECL drivers. This work demonstrated the capabilities of the BiCMOS technology in implementing diversified, high-performance, smart I/O's and voltage referencing circuits.

TABLE I
SUMMARY OF THE POWER COMPONENTS OF THE NEW TRANSCEIVER VERSUS A CML ONE FOR DIFFERENT CONDITIONS

<table>
<thead>
<tr>
<th></th>
<th>Universal Transceiver</th>
<th>Conv_CML</th>
</tr>
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<tbody>
<tr>
<td>Output buffer</td>
<td>UOD1, UOD2</td>
<td>125 mW @ 5V</td>
</tr>
<tr>
<td></td>
<td>75 mW, 80 mW @ 5V</td>
<td>100 mW @ 3.3V</td>
</tr>
<tr>
<td>Input buffer</td>
<td>14.2 mW @ 5 V</td>
<td>21 mW @ 5V</td>
</tr>
<tr>
<td></td>
<td>12.5 mW @ 2V</td>
<td>15 mW @ 3.3V</td>
</tr>
<tr>
<td>Vref Generator</td>
<td>2 mW @ 3.3V</td>
<td>2 mW @ 3.3V</td>
</tr>
<tr>
<td></td>
<td>1/gate</td>
<td>1/gate</td>
</tr>
<tr>
<td>Load Controller</td>
<td>3 mW @ 5V VT &amp; 1.5 mW</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td>1/gate</td>
<td></td>
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REFERENCES


