Low-Power BiCMOS Circuits for High-Speed Interchip Communication

M. S. Elrabaa, M. I. Elmasry, and D. S. Malhi

***Abstract*—A universal BiCMOS low-voltage-swing transceiver (driver/receiver) with low on-chip power consumption is reported. Using a 3.3 V supply, the novel transceiver can drive/receive signals from several low-voltage-swing transceivers with termination voltages ranging from 5 V down to 2 V and frequencies well above 1 GHz. Measured results of test circuits fabricated in 0.8-μm BiCMOS technology are also presented.**

***Index Terms*—BiCMOS integrated circuits, buffers, circuit simulation, current-mode logic, digital integrated circuits, feedback circuits.**

I. Introduction

BICMOS technology has proven to be an excellent workhorse for telecommunication applications [1]. These applications increasingly require higher circuit speeds and higher chip-to-chip bit rates. Also, for ever increasing complexity of telecommunication switches, the need arises for transceivers (driver/receiver) with low on-chip power consumption that can operate at low supply voltages.

Bipolar circuits such as emitter coupled logic (ECL) or current mode logic (CML) can meet the speed requirements at the expense of large power consumption. Different dynamic circuit techniques that reduce the power consumption of ECL/CML logic circuits while maintaining or increasing their speed were recently reported [3]–[6]. However, these techniques were intended for bipolar VLSI logic applications and are not suited for ECL/CML output drivers' applications that have higher current requirements. Recently, many low-voltage-swing driver circuits have been reported. These circuits range from reduced-swing CMOS [7] and CMOS pseudo ECL or CMOS 100 K ECL [8]–[9], to CMOS Gunning transceiver logic (GTL) [10]. The CMOS reduced-swing transceivers have limited speed, and the CMOS true or pseudo ECL are complicated to design and have high power consumption. The GTL requires a special reference voltage. Also, each of these transceivers, as well as the true or pseudo bipolar ECL or CML transceivers, requires a different termination voltage, thus making them incompatible. Signal conversion parts, as well as multiple termination and reference voltages, would be required in systems using parts with different transceiver types, thus increasing the overall system cost and complexity.

Manuscript received May 27, 1995; revised October 17, 1996.

M. S. Elrabaa was with the VLSI Research Group, Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, N2L 3G1, Canada. He is now with Intel Corp., Portland, OR 97124 USA.

M. I. Elmasry is with the VLSI Research Group, Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON, N2L 3G1, Canada.

D. S. Malhi is with the Telecom Microelectronics Center, Northern Telecom Ltd., Ottawa, ON, Canada.

Publisher Item Identifier S 0018-9200(97)02473-6.

In this paper a new universal low-voltage-swing low on-chip power BiCMOS transceiver is presented in Section II. Using a 3.3 V supply, this transceiver can operate with termination voltages ranging from 5 V down to 2 V. The performance of the different building blocks of the new transceiver is evaluated using both simulations and experimental results.

To realize these concepts, these circuits were fabricated in (0.8-μm, 5-V) BiCMOS technology [1], [2] of Northern Telecom with a bipolar junction transistor (BJT) F_t of 12 GHz. These circuits were designed, simulated, and tested at 3.3-V power supply in 5-V technology.

II. The Low-Voltage-Swing Low-Power Universal Transceiver

The novel transceiver consists of a universal receiver and a universal output driver operating at a 3.3-V supply. The receiver can read signals with termination voltages ranging from 1.5 V to 5 V and the driver can drive an external 25 Ω terminated to a termination voltage V_T, ranging from 2 V to 5 V. Neither circuit requires the use of any external reference voltages. However, it is restricted to have level shifting of signals with respect to V_T for this design. Hence, assuming the signal swing V_s to be between 0.8 V to 1.0 V, all signals should be from V_T to $V_T - V_s$.

A. The Universal Receiver

The receiver circuit consists of three subcircuits; the universal input buffer (Fig. 1), the $V_{\rm ref}$ generator [Fig. 2(a)], and the load control circuit [Fig. 2(b)].

1) The Universal Input Buffer (UIB): The UIB is basically an emitter-coupled BJT pair followed by a source-follower stage. Four PMOS devices $M_{1\text{-}4}$ (Fig. 1) are used as loads for the emitter-coupled BJT's. These load devices are controlled by the two biasing voltages, V_1 and V_2, which are generated by the load control circuit. The two PMOS devices, M_5 and M_6, ensure that the n-wells of all the PMOS devices $M_{1\text{-}6}$ are connected to the highest voltage among V_T and $V_{\rm DD}$. The value of the reference voltage $V_{\rm ref}$ in Fig. 1 is kept at about V_T–0.45 V by the $V_{\rm ref}$ generator circuit.

For a termination voltage less than $V_{\rm DD}$ (3.3 V), M_1 and M_4 will be off, and M_2 and M_3 will be on and act as loads for the differential pair. Hence, the output signal of the differential pair will be from $V_{\rm DD}$ to $V_{\rm DD} - V_s$. The n-wells of the PMOS devices $M_{1\text{-}6}$ will be connected to $V_{\rm DD}$ via M_5. Similarly, when V_T is greater than $V_{\rm DD}$, M_2 and M_3 will be off, M_1 and M_4 will be on, and the differential pair output swing will be from V_T to $V_T - V_s$. The PMOS n-wells will be connected to V_T via M_6.

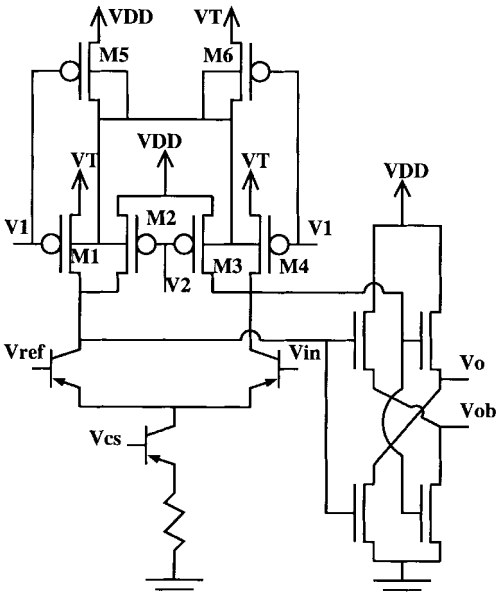

Fig. 1. The universal input buffer (UIB) circuit.

A source-follower stage was used instead of an emitter-follower one to avoid saturating the emitter-follower's BJT's when V_T is larger than $V_{\rm DD}$. This also ensures that the UIB differential output signal will not saturate the input devices of the driven gate. The speed is slightly reduced but the saturation problems are eliminated.

2) The $V_{\rm ref}$ Generator: $V_{\rm ref}$ is about 0.5 $V_{\rm BE}$ below V_T and is generated by the $V_{\rm BE}$ multiplier (made of Q_1, R, and $R/2$). M_{n1} is on only when $V_T \leq 2.5$ V and is used to compensate the decrease in Q_1 current. M_{p1} and the diode are used for temperature compensation. M_{p1} is biased in such a way that its drain current will increase linearly with V_T. This will keep the current through Q_1 constant and hence $V_{\rm ref}$ will always remain constant with respect to V_T. Also, as the temperature increases, the drain current of M_{p1} decreases, and hence, the emitter current of Q_1 will increase and compensate the decrease in $V_{\rm BE}$ that occurs as the temperature increases (which is about -2.5 mV/°C). The reverse happens when the temperature decreases.

Fig. 3 shows the measurement results for the output of the $V_{\rm ref}$ generator versus temperature for several termination voltages. This figure shows the stability of $V_{\rm ref}$ over a wide range of temperatures and termination voltages. The maximum change in $V_{\rm ref}$ over the whole temperature range for all values of termination voltages was about 51 mV (about 5% of the voltage swing).

The measurement results for $V_T - V_{\rm ref}$ versus V_T at room temperature (25°C) are shown in Fig. 4. Two sets of data are shown in that figure. These two sets of data were measured from two randomly selected, different dies that came from two different wafers that were fabricated in two separate runs. This figure shows the accuracy of the generated $V_{\rm ref}$ for various termination voltages and its insensitivity to process. The two data sets are very consistent, and for most values of V_T, the maximum deviation of $V_{\rm ref}$ from the required value is less than 20 mV. The largest deviation in $V_{\rm ref}$ occurred at V_T's between

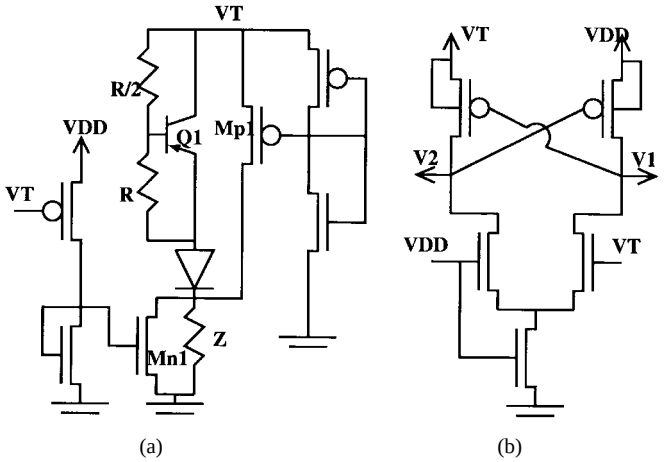

Fig. 2. The two reference circuits used in the universal receiver. (a) The $V_{\rm ref}$ generator. (b) The load control circuit.

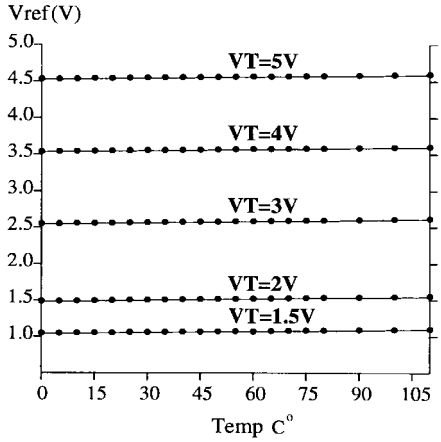

Fig. 3. The measured output of the $V_{\rm ref}$ generator versus temperature for different termination voltages.

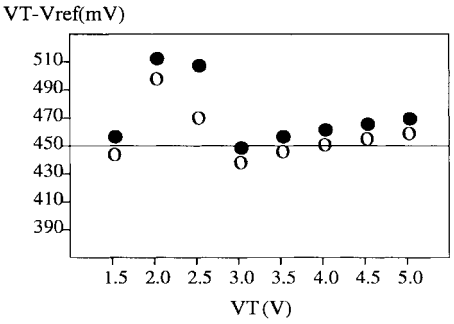

Fig. 4. Measured $V_T - V_{\rm ref}$ room temperature. The data provided is from two wafers fabricated in two different runs.

2 V and 2.5 V, which is the transitional region between the two ranges of operation (above 2.5 V and below 2.5 V) where M_{N1} turns on. However, the deviation is still less than 50 mV and consistent between the two wafers.

3) The Load Control Circuit: This circuit is a simple source-coupled NMOS pair with cross-coupled PMOS loads. The input and load MOS devices are connected and sized in such a way that when V_T is less than $V_{\rm DD}$, V_1 will be "High" and close to $V_{\rm DD}$ (i.e., $V_{\rm DD} - V_1$ would be less than the

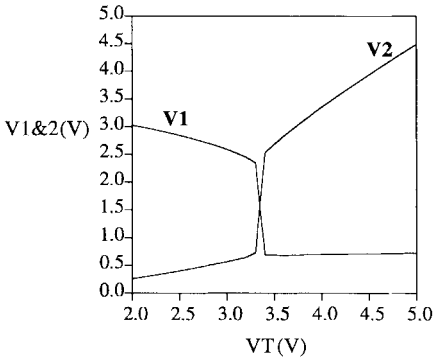

Fig. 5. The outputs of the load control circuit.

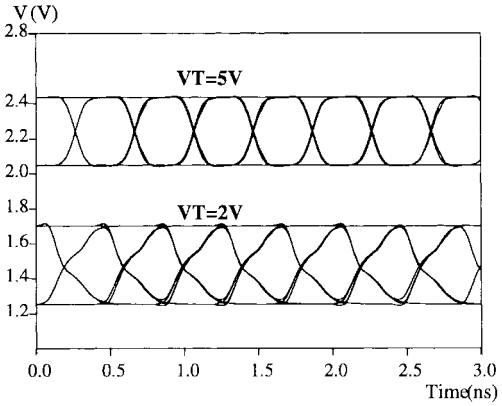

Fig. 6. The simulated eye-diagram for the UIB.

PMOS threshold voltage V_{tp}), and V_2 will be "Low." When V_T is greater than $V_{\rm DD}$, V_2 will be "High" and close to V_T $(V_T - V_2 < V_{tp})$, and V_1 will be "Low."

This ensures the correct operation of the UIB and that no current will be flowing between V_T and $V_{\rm DD}$ under any circumstances.

The outputs V_1 and V_2 versus V_T are shown in Fig. 5. This figure shows the correct operation of the circuit. The load control circuit was found to be very stable over the temperature range. The maximum change in V_1 and V_2 over the temperature range for any value of V_T was found to be less than 10 mV.

4) The Receiver Performance: The simulated eye-diagram of the UIB with a tail current of 1 mA at 1 GHz input frequency is shown in Fig. 6 for two values of V_T (2 and 5 V) and an ECL gate as a fan out. This diagram was generated by applying random 7-b data streams to the UIB's input and overlaying the output responses. As this figure shows, the UIB functions perfectly for the two termination voltages and the intersymbol interference is very minimal.

The measured differential output waveforms of an ECL driver being driven by the new receiver at a frequency of 1.5 GHz are shown in Fig. 7. The receiver's input signal was terminated to 2 V and the UIB's tail current was 1 mA. This shows that the receiver operated at this high frequency and correctly switched the ECL driver. The total power of the receiver was 12.5 mW. Measurements also verified the operation of the receiver for V_{Ts} ranging from 1.5 V to 5 V at this frequency.

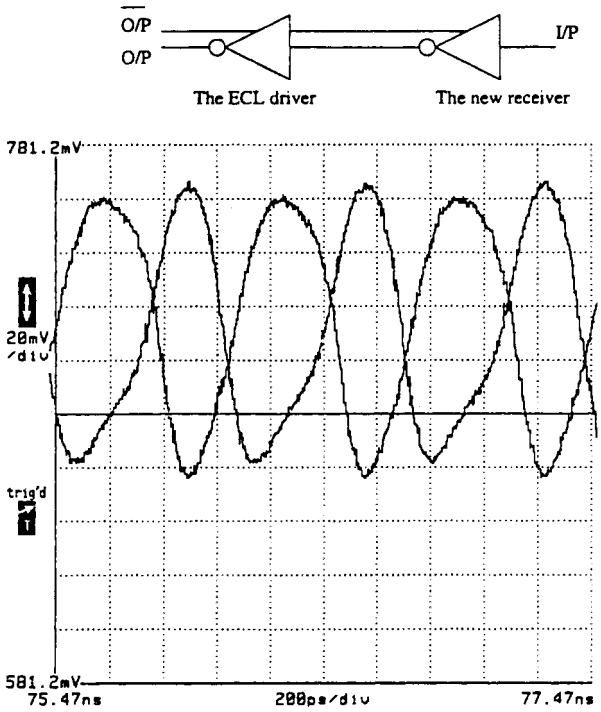

Fig. 7. The output of the receiver test structure at 1.5 GHz and 2 V input signal termination (20 dB attenuation at the inputs of the sampling scope).

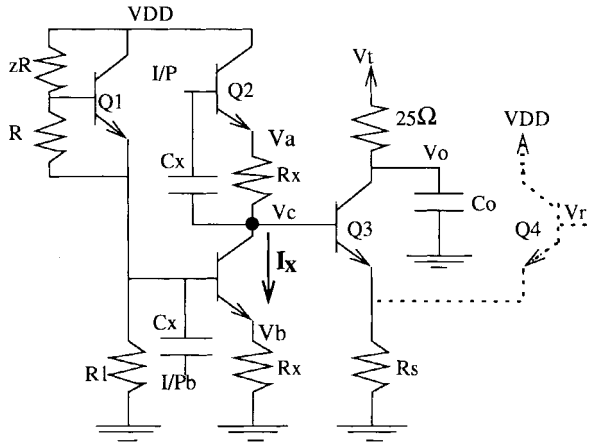

Fig. 8. The two versions of the UOD; the second version UOD2 includes Q_4 (dotted line).

B. The Universal Output Driver (UOD)

Two versions of the universal output driver were developed, Fig. 8. For the design of both drivers, double termination (25 Ω load to V_T) was assumed.

The UOD utilizes a dynamically controlled biasing network to switch a current between two values; a high value when the output is being pulled down and a low value (zero for the UOD1) when the output is being pulled high. Thus, unlike conventional CML drivers, the tail current is turned off when it is not needed.

1) The UOD1: The UOD1 works as follows: The voltage V_c, which in conjunction with R_s determines the value of the tail current, is equal to the difference between the voltages at

V_a and V_b as shown below

$$I_x = \frac{V_b}{R_x} = \frac{V_a - V_c}{R_x}. \quad (1)$$

Hence

$$V_c = V_a - V_b. \quad (2)$$

So when the input I/P is "High" (i.e., $I/P = V_{\rm DD} - V_{\rm BE}$)

$$V_a = V_{\rm DD} - 2 \cdot V_{\rm BE}, \quad V_b = V_{\rm DD} - (1+z)V_{\rm BE}. \quad (3)$$

Hence

$$V_{c_{\rm High}} = V_a - V_b = z \cdot V_{\rm BE} \quad (4)$$

where z is the multiplication factor of the $V_{\rm BE}$ multiplier made of Q_1 and the two resistors R and zR. z was adjusted such that $V_{c_{\rm High}}$ is about 1.2–1.3 V (i.e., z is from 1.5 to 1.8) and R_s was adjusted such that the "High" value of the current is around 32 mA. Also, since V_c (and hence the value of the generated tail current) depends on the difference $V_a - V_b$, the tail current value is independent on supply variations provided that both the predriver and the driver are using the same supply voltage. When I/P is "Low"

$$V_a = V_{\rm DD} - V_{\rm BE} - V_s, \quad V_b = V_{\rm DD} - (1+z)V_{\rm BE} \quad (5)$$

hence V_c becomes

$$V_{c_{\rm Low}} = z \cdot V_{\rm BE} - V_s \quad (6)$$

where V_s is the input voltage swing. The capacitances C_x's are used to enhance the speed and resolve (to some degree) the above tradeoff. Meanwhile, they do not affect the dc characteristics. The following condition is imposed on z to ensure that the "Low" current is zero (when I/P is low V_c would be $\leq V_{\rm BE}$):

$$1 < z \leq 1 + \frac{V_s}{V_{\rm BE}}. \quad (7)$$

Hence, for this driver to be designed properly, a rough value of V_s should be known in advance. The "High" value of the tail current, however, is still independent of the exact value of V_s ($V_{c_{\rm high}} = zV_{\rm BE}$).

This circuit has two shortcomings. 1) The large BJT Q_3 is turned on/off solely through the base. Hence, the base resistance R_B makes the turn-on/off slower than a combined base/emitter turn-on/off (such as in CML/ECL circuits). 2) The "Low" value of the tail current might not be exactly zero although it is designed to be so (it may reach a few hundreds of μA's) due to the tolerance in the resistors in the biasing network. This would slightly reduce the noise margins by reducing the value of V_{oH} (the output high value).

2) The UOD2: To overcome the two shortcomings of the UOD1 mentioned above, the UOD1 circuit was slightly modified to produce the second version of the universal output driver, UOD2 (Fig. 16). A BJT, Q_4 (much smaller than Q_3), is added with its base connected to a voltage reference, V_r, to steer the current when V_c is "Low." Hence, the restriction on z is relaxed ($V_{c_{\rm Low}}$ can be $>V_{\rm BE}$). This increases the speed by making the voltage swing of V_c smaller. Also, when I/P becomes high, the "Low" tail current is steered away from Q_4 to Q_3 and helps in turning Q_3 on faster. The "Low" value of the current is much smaller than the "High" value due to two reasons. 1) V_r is set to a value less than the "High" value of V_c, and 2) since $V_{\rm BE}$ of Q_4 is larger than that of Q_3 (due to the size difference), the voltage drop across R_s is smaller when I/P is low.

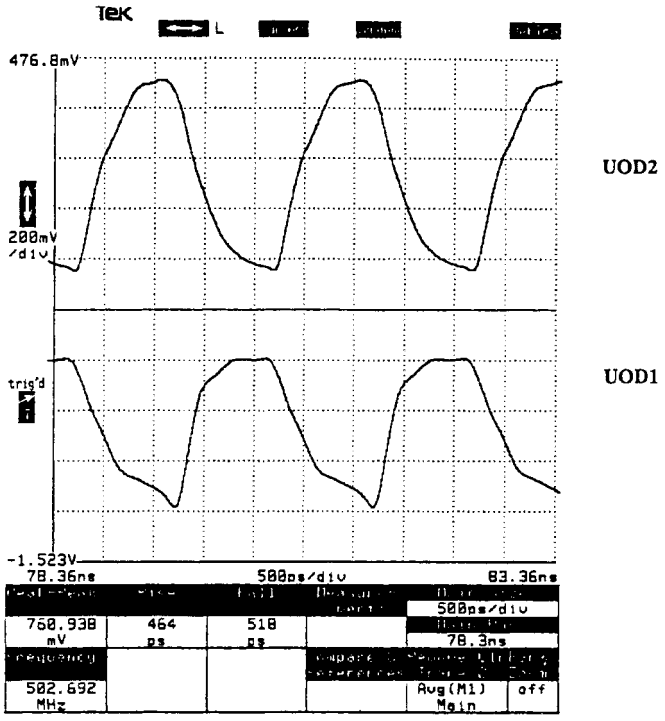

Fig. 9. The outputs of the two UOD's @ 500 MHz and 5 V V_T.

Fig. 9 shows the measured output waveforms of both drivers at 500 MHz and a termination voltage of 5 V. The on-chip powers at that frequency were 75 mW and 80 mW for the UOD1 and the UOD2, respectively. The power of a CML driver at the same termination voltage would be about 125 mW. An ECL or pseudo ECL driver would have an even greater power at the same conditions. For a 2-V termination, the UOD1 and the UOD2 powers are 25 mW and 29 mW, respectively.

Fig. 10 shows the eye-diagram of the UOD2 at 1 GHz. This diagram was generated in a similar manner to that of Fig. 6. As this figure indicates, there is no significant intersymbol interference due to the current switching and the use of decoupling capacitances in these drivers.

Fig. 11 shows the $F_{\rm max}$ of the two drivers (defined as the frequency of operation where the output of the driver drops to 70% of its low-frequency value). It shows superior speed performance of UOD2 over the V_T range. It also shows that for both drivers $F_{\rm max}$ decreases as V_T decreases due to the increase of the collector capacitance and the saturation effects of Q_3. The decrease of UOD2's speed with V_T is faster. Other disadvantages of UOD2 compared to UOD1 are the

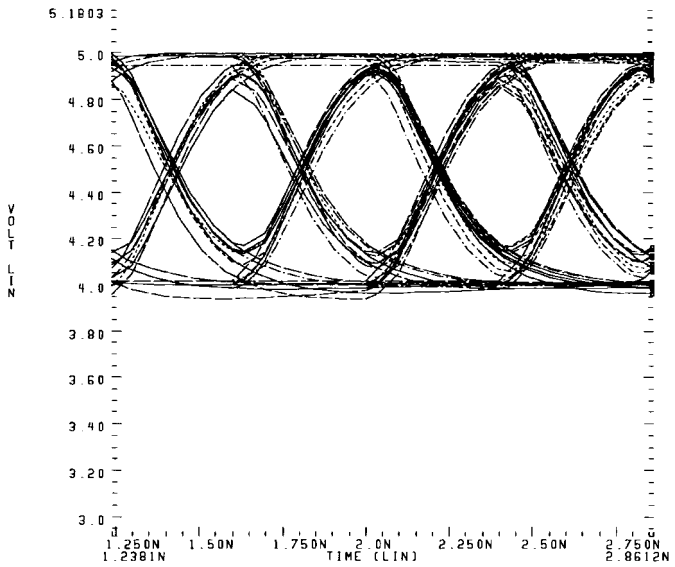

Fig. 10. The eye-diagram of the UOD2 at 1 GHz and 5 V V_T.

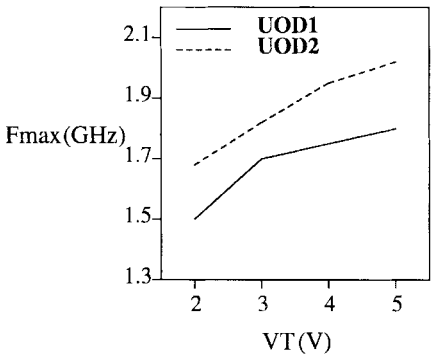

Fig. 11. The simulated maximum frequency of operation of the two UOD's versus V_T.

slight increase in power and area, and the need for an extra reference voltage.

Fig. 12 shows the measured output waveform of the UOD1 at 1 GHz and 5 V termination. This figure shows that the output voltage swing is still 0.8 V (the same as the low-frequency swing) at this high frequency. Table I summarizes the power performance of the new transceivers compared to the conventional CML interface for different conditions. This table shows the superior power performance of the new circuits.

III. Conclusion

Circuit techniques that take advantage of existing BiCMOS technologies and enhance interchip communication were developed. The novel transceiver operated with termination voltages ranging from 2 to 5 V, without the need for an off-chip reference voltage. The good performance of the biasing circuits was demonstrated over a wide range of temperatures and termination voltages. The new drivers would have lower on-chip power than ECL/CML or pseudo ECL drivers. This work demonstrated the capabilities of the BiCMOS technology in implementing diversified, high-performance, smart I/O's and voltage referencing circuits.

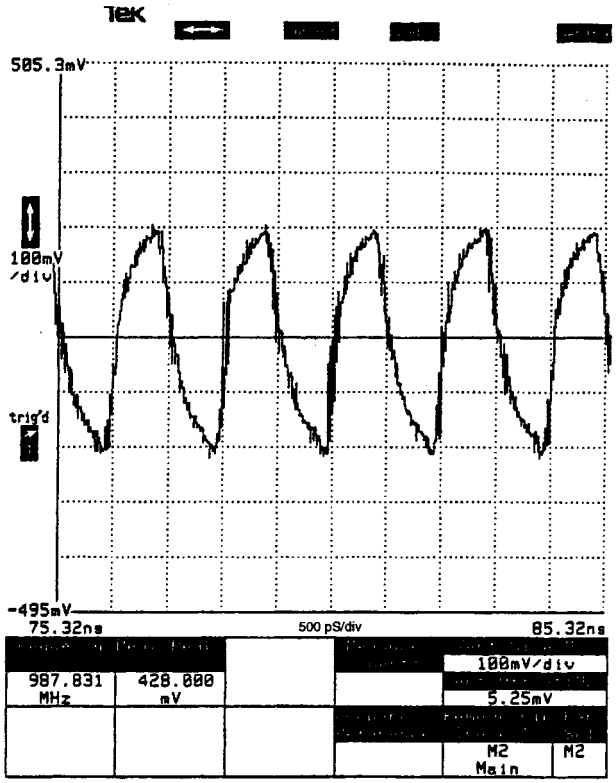

Fig. 12. The output of the UOD1 at 1 GHz and 5 V V_T (6 dB attenuation at the input of the sampling scope).

TABLE I
Summary of the Power Components of the New Transceiver Versus a CML One for Different Conditions

	Universal Transceiver	Conv_CML
Output buffer (Double-termination)	**UOD1, UOD2**	125 mW @ 5V
	75 mW , 80 mW @ 5V	100 mW @ 3.3V
	25 mW, 29 mW @ 2V	50 mW @ 3.3V+
Input buffer	14.2 mW @ 5 V	21 mW @ 5V
	12.5 mW @ 2V	15 mW @ 3.3V
Vref Generator	2 mW @ 3.3V	2 mW @ 3.3V
	1/gate	1/gate
Load Controller	3 mW @ 5V VT & * 1.5 mW @ 2V	N/A

+ single-termination * for any # of gates

Acknowledgment

The authors would like to express their gratitude to NorTel Ltd., Nepean, ON, Canada, for providing fabrication and testing facilities for the circuits reported in this paper.

References

[1] R. Hadaway *et al.*, "BiCMOS technology for telecommunications," in *IEEE BCTM Proc.*, 1993, pp. 159–166.
[2] R. Hadaway *et al.*, "A sub-micron BiCMOS technology for telecommunications," in *Proc. 21st European Solid State Device Research Conf.*, 1991, pp. 513–516.
[3] C. T. Chuang and D. D. Tang, "High-speed low-power AC-coupled complementary push-pull ECL circuit," *IEEE J. Solid-State Circuits*, vol. 27, pp. 660–663, 1992.

[4] C. T. Chuang *et al.*, "High-speed low-power ECL circuit with AC-coupled self-biased dynamic current source and active-pull-down emitter-follower stage," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1207–1210, 1992.
[5] W. Wilhelm and P. Weger, "2 V low-power bipolar logic," in *Proc. ISSCC*, 1994, pp. 94–95.
[6] H. Shin, "A self-biased feedback-controlled pull-down emitter follower for high-speed low-power bipolar logic circuits," *IEEE J. Solid-State Circuits*, vol. 29, pp. 523–528, 1994.
[7] J. H. Quigley *et al.*, "Current mode transceiver logic (CMTL) for reduced swing CMOS, chip to chip communication," in *IEEE Int. ASIC Conf. & Exhibit Proc.*, 1993, pp. 452–455.
[8] M. Pedersen and P. Metz, "A CMOS to 100 K ECL interface circuit," in *ISSCC Tech. Dig.*, pp. 226–227, 1989.
[9] T. J. Gabara and S. Knauer, "Digital transistor sizing techniques applied to 100 K ECL CMOS output buffers," in *IEEE Int. ASIC Conf. & Exhibit Proc.*, 1993, pp. 456–459.
[10] B. Gunning *et al.*, "A CMOS low-voltage-swing transmission-line transceiver," in *ISSCC Tech. Dig.*, 1992, pp. 58–59.