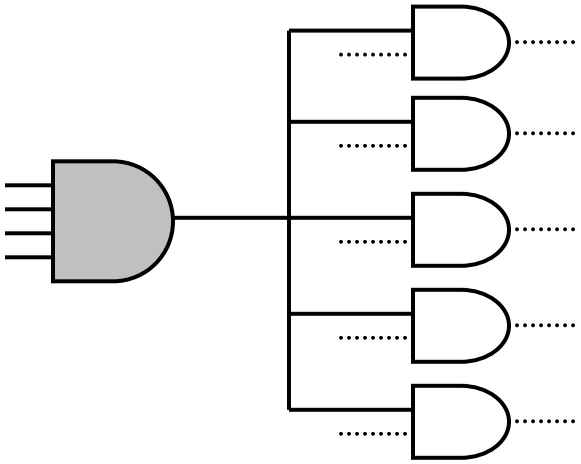
Review of Basic Digital Integrated Circuits Concepts

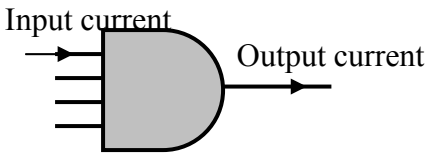
Handouts by Dr. Muhammad Elrabaa for COE360

1. **Fan in:** Is the number of inputs of a digital gates
2. **Fan out:** Is the number of gates' inputs connected to the output of a gate (the amount of loading). Sometimes the other types of loads (wires, pads, etc.) are expressed as fan out equivalent.

Example: For the following gate the Fan in is **4** and the Fan out is **5**.

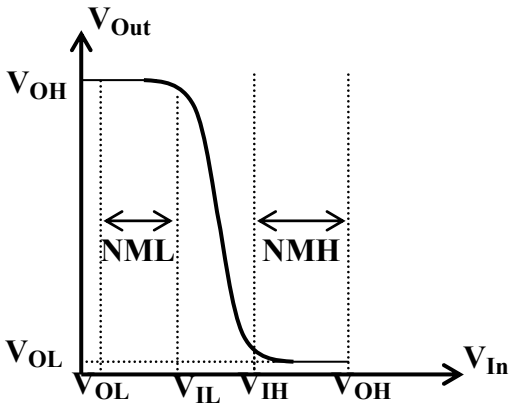


3. **Input & Output Currents:**
   - **a.** $\mathbf{I_{IL}}$ is the input current to a gate when the input has a logic value of 0 (low input current)
   - **b.** $\mathbf{I_{IH}}$ is the input current to a gate when the input has a logic value of 1 (high input current)
   - **c.** $\mathbf{I_{OL}}$ is the output current of a gate when the output has a logic value of 0 (low output current)
   - **d.** $\mathbf{I_{OH}}$ is the output current of a gate when the output has a logic value of 1 (high output current)



4. **Noise Margins:** These circuit parameters specify the circuit's ability to withstand noise.
   - **a.** **The low noise margin (NML or NM0)** specifies by how much an input voltage representing logic 0 can change before an error occurs due to it being interpreted as 1.
   - **b.** **The high noise margin (NMH or NM1)** specifies by how much an input voltage representing logic 1 can change before an error occurs due to it being interpreted as 0.

A typical voltage characteristic (output voltage versus input voltage) of a digital gate is shown below.



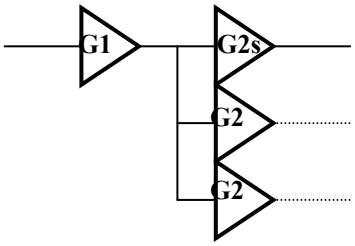
V_{OH} is the high output level
V_{OL} is the low output level
V_{IL} is the maximum low (logic 0) input voltage
V_{IH} is the minimum high (logic 1) input voltage

$NML = V_{IL} - V_{OL}$

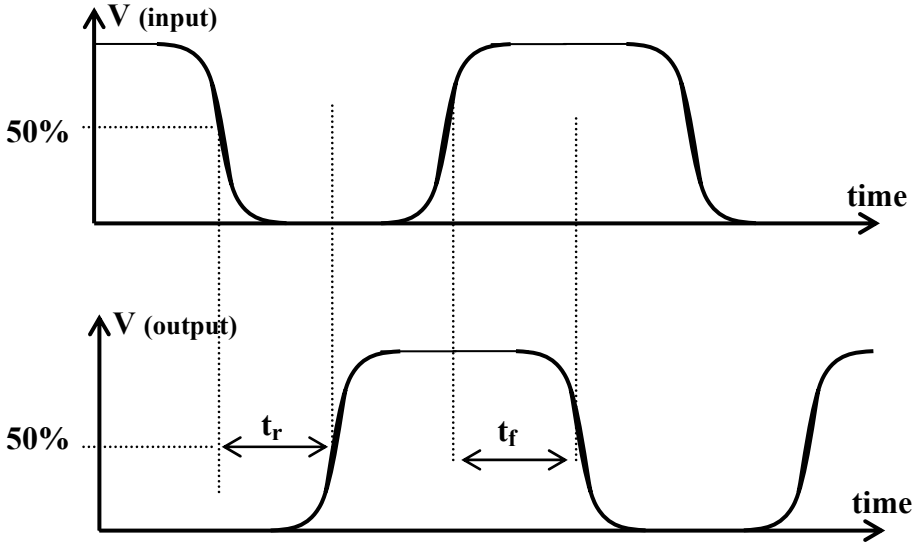
$NMH = V_{OH} - V_{IH}$

For these gates to operate properly,

V_{OL} of G1 should be < V_{IL} of G2 &
V_{OH} of G1 should be > V_{IH} of G2 &
I_{OH} of G1 should be > 3 x I_{IH} of G2 &
I_{OL} of G1 should be > 3 x I_{IL} of G2



5. **Propagation Delay:** The figure below shows the input and output waveforms of a digital gate where all the delay parameters are defined on the figure.



Average propagation delay $T_D = (t_r + t_f)/2$

6. **Power Dissipation:** In general, the amount of power dissipated by a logic gate has two components a static one and a dynamic one.
   - **a.** Static Power (P_{St}) is due to DC current flow between the two supplies (VDD and ground) and = I_{DC} x VDD
   - **b.** Dynamic Power is due to the charging and discharging of capacitances at the outputs of the gates. These capacitances are made of wiring capacitances, capacitances of the output transistors of the gate itself, and input capacitances of the gates connected to the output of the gate (the Fan out). The average value of the dynamic power $P_D = f \times C \times VDD^2$ where f is the switching frequency in hertz and C is the output (load) capacitance.

Total power $P_T = P_{St} + P_D$.