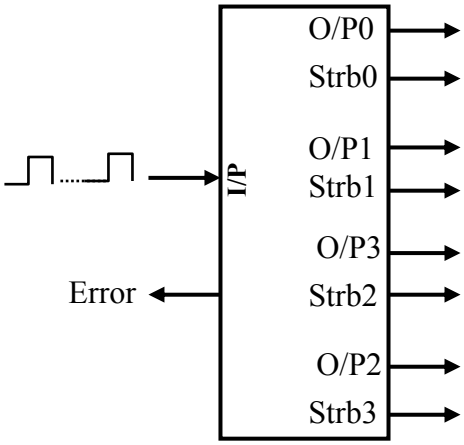
COE360 Course Project (061)
Dr. Muhammad Elrabaa

Implement one of the following projects using AMI's 0.35 μm technology (3.3V supply) and assume 2 pF load capacitance at all your circuit's outputs. Also, all gates should have symmetrical noise margins.

I. For Groups of 3 students:

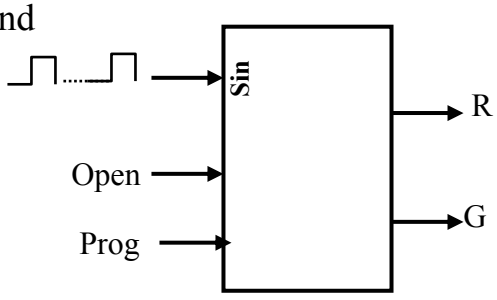
Design a simple switch with one serial input port and 4 parallel output ports. The switch detects the start of the serial input data by 2 start bits (00, 01, 10 or 11). Data is received serially as packets of 8 bits (7 data bits + 1 Parity bit) at a data rate of 1.25 GBPS with two start bits (11 or 00). A stop bit (0 or 1) is used to indicate the end of data and continuation bit (1 or 0) is inserted between packets. The 1st 2 data bits in the 1st packet specify the output port. Data is outputted in parallel to the output ports (i.e. 8 bits wide) with a strobe signal (Strb). An error signal is activated if the parity bit does not match the data.



II. For Groups of 2 students:

Design a digital lock circuit. The circuit receives serial input combinations (one bit at a time). If they match a 6-BCD Digits stored pattern, the lock is enabled. Also, the user can store a new pattern (i.e. re-program the lock).

The circuit should operate at 1.25 GHz. If 3 wrong combinations are entered in a row, the lock jams and would need to be reset. The Lock has 3 I/Ps; Program, Open, and Serial input.
It has two O/Ps; Red and Green.
If the lock is opened, the Green is on.
If it is locked the Red is ON.
If it is gammed both Red and Green are ON.



The deliverables for this project are as follows:

1. **Phase I: Logic Design** **Due Wed 15/11/2006**

   This is the gate level implementation of the project. This part should include logic verification (e.g. using Logic Works or HDL).

2. **Phase II: Circuit Design** **Due Saturday 16/12/2006**

   This is the transistor level implementation of the project. This part includes all the SPICE files simulation results.

3. **Phase III: Mask Design (layout)** **Due Wed. 17/1/2007**

   This is the physical mask level (i.e. layout) implementation of the project. It includes the post-layout verification using IRsim and SPICE simulations. All layouts should be DRC clean and clearly labeled. A short final report documenting the whole project should be submitted and an exit interview shall be conducted.