# COE360 Course Project
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Choose one of the following projects depending on your group size. For all projects use AMI's 0.5 µm technology (5V supply) and assume 2 pF load capacitance at all your circuit's outputs. Also, all gates should have symmetrical noise margins and rise and fall times

I. **Projects for Groups of 3:**

1. Design an 8-bit X 8 FIFO buffer that can be read and written simultaneously with a buffer full/empty indicators and operating frequency of 500 MHz.
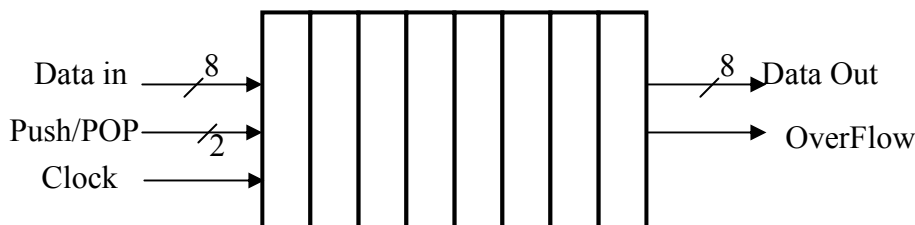
2. Design a digital filter that implement the function at 500 MHz:

$$Y = \sum 2^i X_i \ , \qquad i=1,2,3$$

   The input data (X) are 6-bit signed-integers. Round the results to produce an 8-bit signed-integer result.

3. Design a small look-up table (4 lines, 24-bits wide). An 8-bit word is read with a 16-bit tag, if the entry exists, otherwise a miss indicator is asserted. New entries are always written over the oldest-read entry. Operating frequency is 250 MHz.

II. **Projects for Groups of 2:**

4. Design a 6-bit pipelined parallel multiplier with a clock frequency of 800 MHz.

5. Design a circuit that counts the occurrence of a certain pattern in an input bit stream. The circuit should be resetable and able to count up to 255 patterns at an input bit frequency of 500 Mbps.

6. Design a serial-to-parallel data converter. The input stream is 500 Mbps and the output is 8-bit wide.

The deliverables for this project are as follows:

1. **Phase I: Logic Design   Due Monday 10/11/2003**

   This is the gate level implementation of the project. This part should include logic verification (e.g. using Logic Works or HDL).

2. **Phase II: Circuit Design   Due Wednesday 10/12/2003**

   This is the transistor level implementation of the project. This part includes all the SPICE files simulation results.

3. **Phase III: Mask Design (layout)   Due Monday 5/1/2004**

   This is the physical mask level (i.e. layout) implementation of the project. It includes the post-layout verification using IRsim and SPICE simulations. All layouts should be DRC clean and clearly labeled. A short final report documenting the whole project should be submitted and an <u>exit interview</u> shall be conducted.