COE 200, Term 042

Fundamentals of Computer Engineering

HW# 8

Q.1. Using minimum number of gates and Full-Adders design a circuit that multiplies an 8-bit number X by 10.
Hint: *10*X = 8*X + 2*X*

Q.2. Implement a 4-to-16 Decoder using the minimum number of 2-to-4 decoders with enable inputs. If the resulting 4-to-16 Decoder is to be provided with an enable input En, show the modified circuit.

Q.3. Implement the following functions using minimum-sized Decoders and minimum number of extra gates:

a. F(X,Y,Z) = XY + Z
b. F(A,B,C,D) = D(A` + B)
c. F(X,Y,Z) = X`(Y` + Z`) + YZ`
d. F(X,Y,Z) = X`(Y` + Z`) + XZ
e. F(A,B,C) = A`
f. F(A,B,C,D,E) = 1
g. F(A,B,C,D,E,G,H) = 0
h. F(X,Y,Z) = $\sum$ (0,3,5,6) , d(X,Y,Z) = $\sum$ (1,2,4,7)
i. F(A,B,C,D) = Π(1,7,9,13,15)

Q.4. Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable input and one 2-to-4 line decoder.

Q.5. A Combinational circuit is defined by the following three Boolean functions:

$F_1(X, Y, Z) = X`Y` + XYZ`$
$F_2(X, Y, Z) = X` + Z$
$F_3(X, Y, Z) = XY + X`Y`$

Design the circuit with a 3x8 decoder, four 2-input OR gates, and an inverter.