COE 200, Term 042

Fundamentals of Computer Engineering

HW# 4

Q.1. A majority gate is a digital circuit whose output is equal to 1 if the majority of inputs are 1`s. The output is 0 otherwise.

(i) By means of a truth table, find the Boolean function implemented by a 3-input majority gate.

(ii) Express the 3-input majority gate as a sum of minterms and a product of maxterms.

Q.2. Express the following functions in a sum of minterms and a product of maxterms :

(i) F(X,Y,Z) = (XY + Z)(Y + XZ)

(ii) F(A,B,C,D) = D(A` + B) + B`D

(iii) F(A,B,C) = AB + AC + A`B` + B`C`

(iv) F(A,B,C) = (A+B+C)(A`+B`)

Q.3. Find the minterms and maxterms of the complement of the functions specified below:

(i) F(X,Y,Z) = $\sum$(0,2,4)

(ii) F(A,B,C,D) = Π(1,7,9,13,15)

Q.4. For the Boolean function E and F, as given in the following truth table:

X	Y	Z	E	F
0	0	0	1	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	0	1

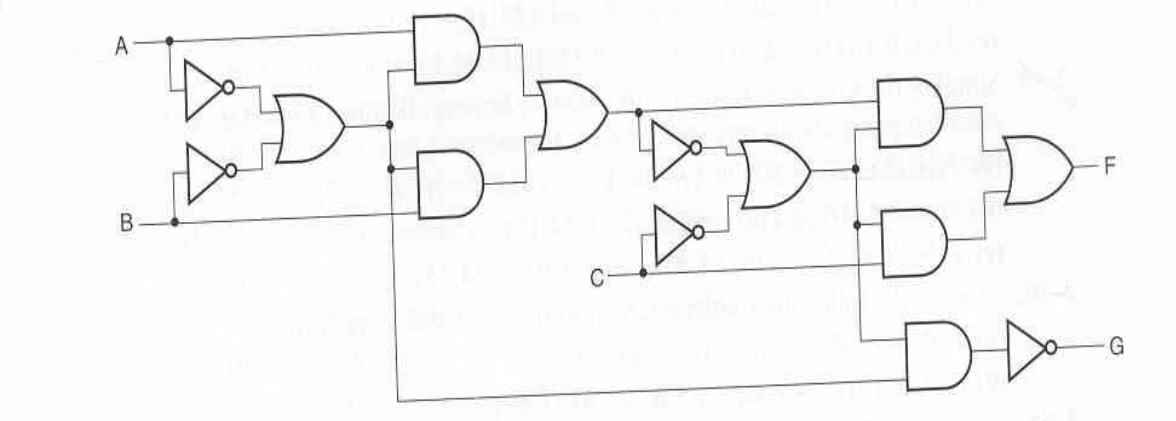
(i) List the minterms and the maxterms of each function.

(ii) List the minterms of E' and F'.

(iii) List the minterms of E + F and E . F.

(iv) Express E and F in sum-of-minterms and product-of-maxterms algebraic form.

Q.5. Consider the circuit shown below:



(i) Assuming that the propagation delay of an INVERTER is 1ns, a 2-input AND gate is 2ns and a 2-input OR gate is 2ns. Compute the largest propagation delay in this circuit and determine the critical path i.e. the path that has the largest propagation delay.

(ii) Determine the smallest propagation delay in this circuit and the input conditions under which this delay occurs.

(iii) What is the fanout of the first OR gate in the circuit. What is the smallest and largest fanout in the circuit.

(iv) Assume that you have initially A=0, B=0, C=1. Draw the timing diagram showing the change in F and G as a result of changing A from 0 to 1 while keeping the assignment of B and C.