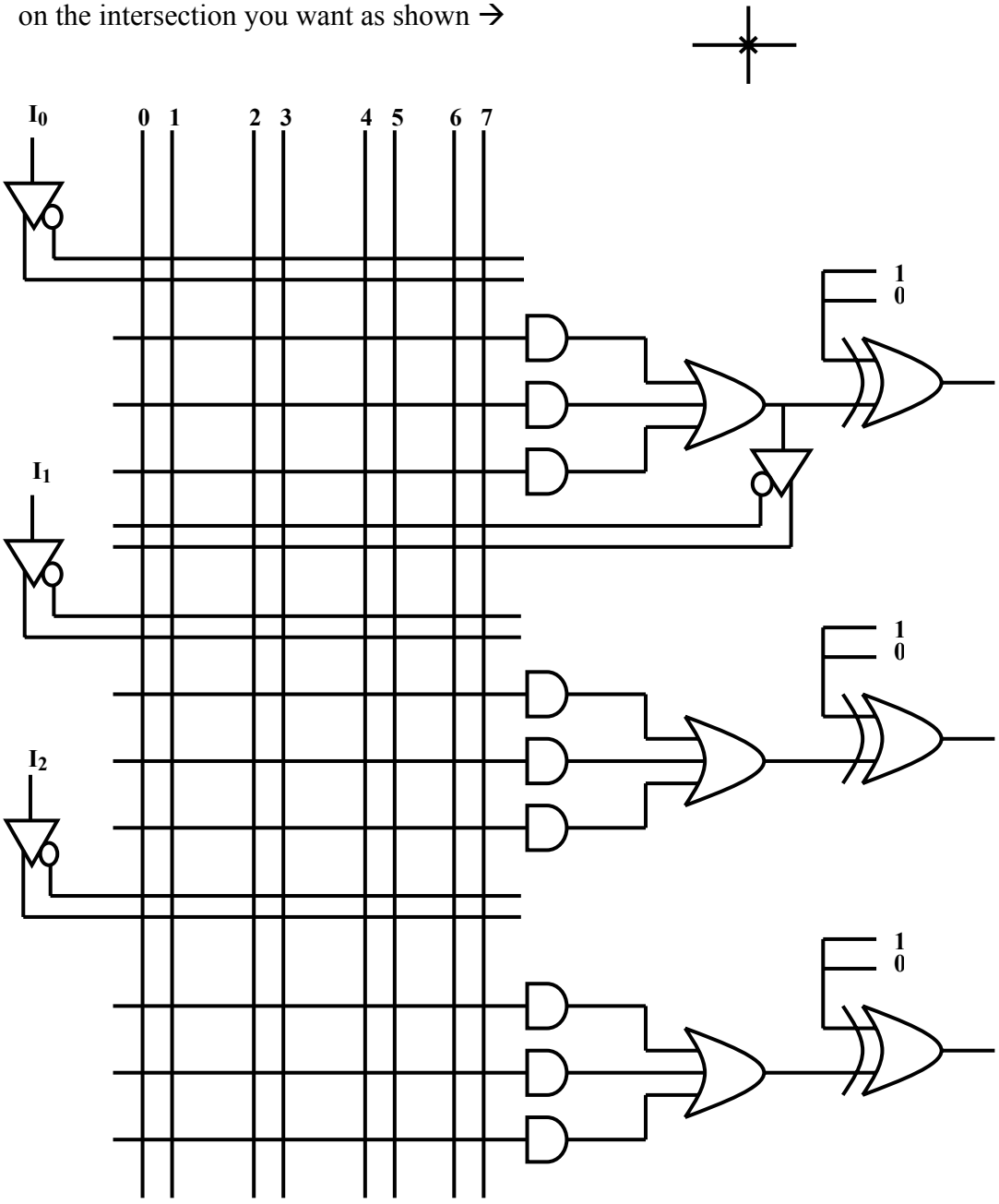
COE 200, Term 051

Fundamentals of Computer Engineering

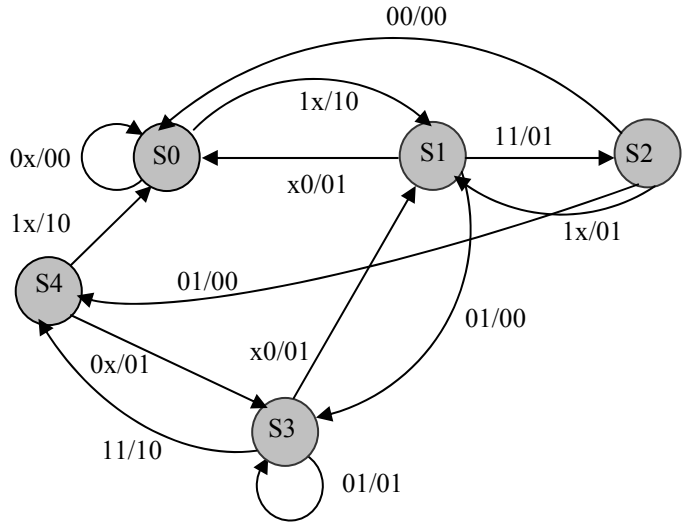
HW# 12

Q.1. Using the PAL shown below to implement the following functions:
$F_1(A,B,C) = \Pi\ (2, 3, 4,7)$, $F_2(A, B, C) = \sum (0,1,5)$

Show your solution on the diagram below directly. Indicate connections by placing an x on the intersection you want as shown →



Q.2. It is required to design a sequential circuit that has the state diagram shown below:



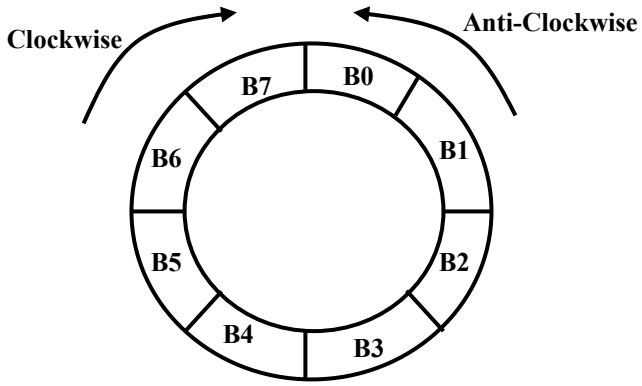
(i) Implement the sequential circuit using D-FFs and the smallest number of gates possible using binary state assignment.

(ii) Implement the sequential circuit using D-FFs and the smallest sized ROM possible.

(iii) Implement the sequential circuit using DF-FFs and the smallest number of gates possible using One-Hot state encoding.

Q.3. Design an 8-bit rotator (A shift register with both ends tied together as shown below) with two control inputs S1 and S0. The table below summarizes the required functionality:

S1 S0	Function
0 0	**Stay the same**
0 1	**Rotate Clockwise 1-bit (B7→B0, B0→B1, B1→B2 …B6→B7)**
1 0	**Rotate Anti-Clockwise 1-bit (B0→B7, B1→B0, B2→B1 …B7→B6)**
1 1	**Clear register (B7,6,5..0 ← 0)**



Show how would you change your design to make the rotation 2-bits (i.e. B7→B1, B0→B2, B1→B3 …B6→B0)?

Q.4. Design a 4-bit synchronous counter (outputs $Q_3Q_2Q_1Q_0$) using D-FFs that two control inputs with the following functionality:

S1 S0	Function
0 0	**Stay the same**
0 1	**Count-Up at a step of 2 (0000 → 0010 → … or 0001 →0011 → 0101 ...)**
1 0	**Count-Down at a step of 2 (0000 → 1110 → 1100 →… or 0001 →1111 → 1101 ...)**
1 1	**Parallel load**

Hint: Notice the following: When the present state (i.e. the present value of $Q_3Q_2Q_1Q_0$) is even, then when we are counting up Q_0=0, while Q_1 toggles every time, Q_2 toggles when Q_1=1, and Q_3 toggles when $Q_2 \cdot Q_1$=1.

Similarly you can obtain the remaining conditions (counting down starting from an even number, or counting up/down starting from an odd number)

Q.5. It is required to design a circuit that reads data serially, adds a constant number(7-bits) to it and then output it in parallel (8-bits) along with a strobe signal. The data format is as follows; 2 start bits (two 1s), a single stop bit (0) and the data packets (each is 7-bits long) are separated by a single 1 (continuation bit). When there is no data on the input it is kept low (i.e. 0). The circuit should be fully synchronous with an external clock and have a master asynchronous reset input. The diagram below shows the block diagram of the circuit and the data format.

Obtain the data path and control units for this circuit using D0FFs and any other components you like.