COE 200, Term 042

Fundamentals of Computer Engineering

HW# 10

Memory Elements Design & Operation

Q.1. Draw the logic diagram of a clocked D-Latch using NOR gates only.

Q.2. Show the design of the following flip-flops using SR latches and external gates:

(i) A negative-edge triggered D-FF.

(ii) A negative edge-triggered JK-FF.

(iii) A positive-edge triggered T-FF.

Q.3. A set-dominant flip-flop has set and reset inputs. It differs from a conventional SR flip-flop in that, when both S and R are equal to 1, the flip-flop is set.

(i) Obtain the characteristic table of the set-dominant flip-flop.

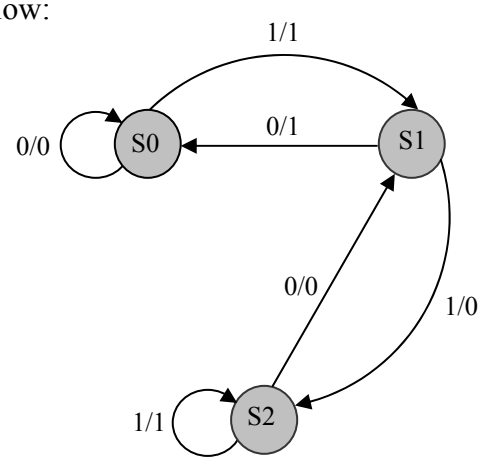
(ii) Derive the excitation table for the set-dominant flip-flop.

(iii) Design a positive-edge triggered set-dominant flip-flop using D-FF.

(iv) Design a positive-edge triggered set-dominant flip-flop using JK-FF.

Synchronous Sequential Circuit Design

Q.4. It is required to design a sequential circuit that receives a serial input X, and produces a serial output Z, equivalent to 3*X, i.e., Z=3*X. The state diagram for this circuit is shown below:



(i) Implement the sequential circuit using D-FFs and the smallest number of gates possible assuming the state assignment: S0=00, S1=01, and S2=10.

(ii) Implement the sequential circuit using D-FFs and the smallest number of gates possible assuming the state assignment: S0=11, S1=01, and S2=10.

(iii) Implement the sequential circuit using JK-FFs and the smallest number of gates possible assuming the state assignment: S0=00, S1=01, and S2=10.

Q.5. You are to design a serial adder (**Add3**) that computes the sum of three separate serial input streams rather than the usual two. The adder has three primary inputs X_1, X_2, X_3, and a single primary output Z. Draw the state diagram, construct the state table, and use D flip-flops and show the detailed design of the **Add3**.

Q.6. A sequential circuit **MON** is to be designed to monitor the condition of a patient in a hospital bed. The input to **MON** is a binary number *n* that ranges in value from 1 to 7 and indicates the patient's condition. The expected value of *n* is sent to **MON** automatically every five seconds. If *n* goes below **2** or above **4** on *two or more* occasions, the machine should activate an alarm at a nurse's station. The nurse responds by administering medication to the patient and resetting the monitor. *Using JK flip-flops and NOR* gates only, carry out the logic design of **MON**. Obtain a state table, a state assignment, and a complete logic diagram.

Synchronous Sequential Circuit Analysis

Q.7. A sequential circuit uses 2 flip-flops. The first (**A**) is a **D-FF** while the second (**B) is a JK-FF**. The circuit has 2 inputs X and Y, and one output Z. The circuit is specified by the following input equations:

$D_A = X` Y + X A$ $\quad J_B = X` B + X A$ $\quad K_B = X` A + X B$ $\quad Z = B$

(i) Draw the logic diagram of the circuit.

(ii) Derive the state table.

Additional Design Problem

Q.8. Design a sequential circuit with two flip-flops A and B and two inputs E and X. If E=0, the circuit remains in the same state, regardless of the value of X. When E=1 and X=1, the circuit goes through the state transitions from 00 to 01 to 10 to 11, back to 00, and then repeats. When E=1 and X=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01, back to 00, and then repeats. Design the circuit using the following types of FFs:

(i) Positive-edge-triggered D-FF.

(ii) Positive-edge-triggered JK-FF.

(iii) Positive-edge-triggered T-FF.