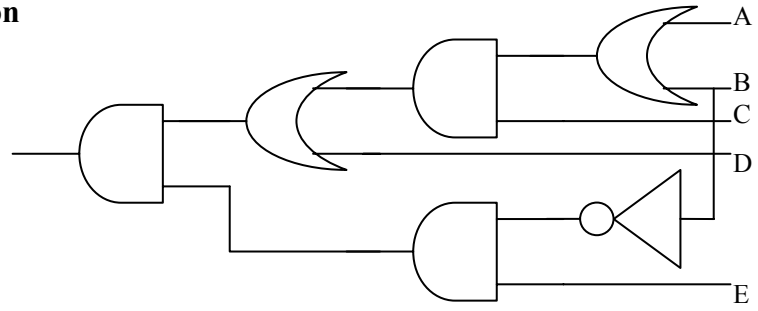
Q.1. Convert the following logic diagram to:

(a) NAND Only implementation
(b) NOR Only implementation



Q.2. Implement the following functions, assuming the inputs are only available in true format and using the specified conditions:

(i) $F = \overline{(XY + Z)}(Y` + XZ)$ Using minimum number of logic levels and using NANDs only

(ii) Repeat (i) above using minimum number of NAND gates

(iii) $F = \overline{(XY + ZY`)}\, X`Z`$ Using minimum number of logic levels and using NORs only

(iv) Repeat (iii) above using minimum number of NOR gates

Q.3. A combinational circuit has 4 inputs (X, Y, W and Z) and one output. The output is 1 if the majority of inputs are equal to 1 and it is 0 otherwise. Show the implementation of this circuit using:

(i) An 8-to-1 Multiplexer,

(ii) Minimum number of 3-to-8 decoders,

(iii) Minimum number of 2-input NAND gates.

Q.4. It is required to design a circuit that has two 4-bit inputs $\mathbf{A=A_3A_2A_1A_0}$ and $\mathbf{B=B_3B_2B_1B_0}$ and one 5-bit output $\mathbf{C=C_4C_3C_2C_1C_0}$. The circuit implements the following four functions based on the values of the two selection inputs, S1 and S0.

S1 S0	Function
0 0	C=A - B
0 1	C=A + B
1 0	C=-A
1 1	C=2A

Implement the circuit using any components you like (including MSI components).