KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 202: Fundamentals of Computer Engineering
Term 111 (Fall 2011)

Instructor: Dr. Abdulaziz Barnawi
Lecture: U.T.: 8:30-9:45 AM
Class location: Bldg. 24-156
Office hours: S.M.: 11:00-11:50 AM, T.: 1:00-1:50 PM, or by appointment
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Course Description:
Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuits analysis and design, multiplexers, decoders and adders. Sequential circuit analysis and design, basic flip-flops, clocking and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations.

Pre-requisite: PHSY 102 - General Physics II

Textbook:
Logic and Computer Design Fundamentals, Morris Mano and Charles Kime, Fourth Edition, Prentice Hall International, 2008.

Tentative Grading Policy:

Homework Assignments	10%	
Quizzes	10%	
CAD Assignments	05%	
Major Exam I	20%	(Tentative: Thu. 13 October 2011, Evening)
Major Exam II	25%	(Tentative: Thu. 8 December 2011, Evening)
Final Exam	30%	
Bonus for100% attendance	03%	

IMPORTANT NOTES:

- All KFUPM regulations and standards will be enforced. Attendance will be checked each class. The KFUPM rule pertaining to a DN grade will be strictly enforced (i.e. **> 6 absences** will result in a DN grade).
- Prompt attendance in classes shows how keen you are to benefit from this course and enhances your performance and grade. Therefore, three late attendances are counted as one absent.
- Only university approved/certified excuses will be accepted, and should be presented **no later than 1 week** after absence.
- Assignments are submitted **at the beginning of class** at the due date.
- You have 48 hours to object to the grade of homework, a quiz, or a major exam from the end of the class time in which the graded papers have been distributed back.
- Check the course webpage and your Blackboard for updates, emails and announcements.
- *Check your exam schedule carefully*. **NO make up exams without an official excuse that includes Exams**. **You must inform the instructor on the same day of missed exam/quiz.**

Course Objectives:

After successfully completing the course, students will be able to:

1. Use math and Boolean algebra in performing computations in various number systems and simplification of Boolean algebraic expressions.
2. Design efficient combinational and sequential logic circuit implementations from functional description of digital systems.
3. Use CAD tools to simulate and verify logic circuits.

Course Learning Outcomes:

Course Learning Outcomes	Outcome Indicators and Details	Assessment Methods and Metrics	Min. Weight	ABET 2000
Ability to use math and Boolean algebra in performing computations in various number systems and simplification of Boolean algebraic expressions.	• Represent integer and fractional values in various number systems • Convert number representation from one system to another • Perform arithmetic operations in various number systems • Represent data in different binary codes including error detecting codes • Simplify Boolean expressions using Boolean algebra & identities	• Quizzes • Assignments • Exams	20%	A(H)
Ability to design efficient combinational and sequential logic circuit implementations from functional description of digital systems.	• Derive gate-level implementation of a given Boolean expression and vice versa • Ability to build larger combinational functions using predefined modules (e.g., decoders, multiplexers, adders, Magnitude comparators.) • Ability to build a state diagram / table for both Moore & Mealy models from functional description • Ability to design & implement Moore & Mealy model synchronous sequential circuits using different Flip-Flop types. • Ability to draw timing diagrams for major signals of both sequential and combination circuits	• Quizzes • Assignments • Exams	50%	C(H)
Ability to use CAD tools to simulate and verify logic circuits.	• Ability to simulate and verify the operation of combinational circuits • Ability to simulate and verify the operation of sequential circuits	• Assignments	5%	K(L)

Tentative Class and Lab Schedule

Week	Topics
1	• Introduction. Information Processing, and representation. Digital vs. Analog quantities. Number systems: Binary system. • Weighted Number Systems. Decimal, Binary, Octal and Hexadecimal. • Arithmetic in Binary and Hex (addition, subtraction& Multiplication) • Number base conversion (Dec to Bin, Oct, and Hex, General). Conversion (Bin to OCT, Hex).
2	• Decimal Codes: BCD, Excess-3, other codes, Parity Bits. • Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra. Principle of duality. • DeMorgan's law, Algebraic manipulation. • Gate Implementation of Boolean expressions
3	• Canonical and Standard forms, Minterms, Maxterms, Sum of products & Products of Sums. • 2-Level gate implementation SOP, POS, AOI, OAI), and multi-level logic. • From Truth tables to Boolean Expressions • Physical properties of gates: fan-in, fan-out, propagation delay. Timing diagrams. Tri-state drivers.
4	• ***Map method of simplification***: Two-, and Three-variable K-Map. • POS simplification • Don't care conditions and simplification.
	Major I (Thursday 13 October)
5	• **Universal gates (NAND, NOR)** • ***Implementation using NAND and NOR gates:*** 2-level & multilevel implementation. • Exclusive-OR (XOR) and Equivalence (XNOR) gates, Odd and Even Functions, Parity generation and checking.
6	• Combinational Circuit Design Procedure & Examples: o Code Converter. o BCD to 7-Segment Display Conversion o Half and Full Adders,

7	○ Ripple Carry Adder design • ***Delay*** analysis of RCA • Signed Numbers: sign-magnitude, 1`s complement, and 2`s complement. • Signed Binary Arithmetic. (Addition and Subtraction in 2`s complement). • Binary Adder-Subtractor. • Carry Look-ahead adder. • ***Delay*** analysis
8-9	• Decoders 2x4, 3x8, 4x16. Designing large decoders from smaller decoders. Function implementation using decoders. • Encoders: Priority Encoders. Applications of decoders and priority encoders. • Multiplexers**:** 2x1, 4x1. Constructing large MUXs from smaller ones. Function implementation using multiplexers. • Function implementation using multiplexers. • Magnitude Comparator • MSI Design Examples
	Major 2 (Thursday 8 December)
10	• ***Sequential Circuits:*** Latches, Clocked latches: SR, D, T and JK. Race problem in clocked JK-Latch. . • ***Flip-Flops:*** Master-Slave, D-FF. • Designing flip-flops from D-FF.
11	• *Asynchronous/Direct Clear and Set Inputs.* Setup, Hold, FF propagation delay. • *Sequential Circuit Design*. Design procedure, State diagrams and state tables. • Analysis of Sequential Circuits. State table, State diagram.
12	• Registers, Registers with parallel load. • Synchronous Binary Counters*:* Up-Down Counters • Counters with Parallel load, enable, synchronous clear and asynchronous clear. • Use of available counters to build counters of different count. • Design with unused States • Shift Registers. Bi-directional shift register.
13	• Mealy vs. Moore machine. • The workings of a state machine as to when do states and outputs change w.r.t changes in the clock and the presented inputs should be stressed • Design Examples and Calculation of maximum clock frequency.
14	• Memory devices: RAMs & ROMs. • Combinational Circuit Implementation with ROM. • Sequential Circuit Implementation using ROMs. • Programmable Logic Devices: PLAs, PALs, FPGA’a. • ***Review***