Timing Diagrams

Please refer to textbook page 49. Usually the low voltage level (i.e. 0 volts) is considered 0 binary while the high voltage level (i.e. 3 or 5 volts) is considered as 1 binary.

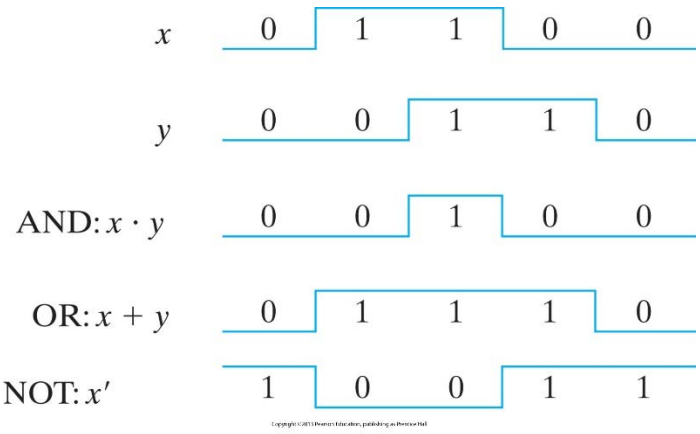
Example 1:

Given the timing signal for x and y as shown in Figure, draw the timing signal for

a) x.y
b) x+y
c) x'

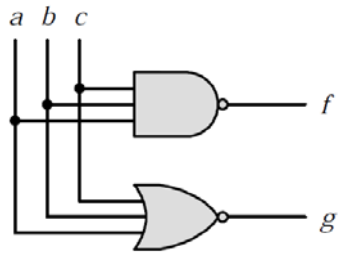
solution:

In this example we ARE GIVEN EXPLICITY the signals x and y. We are asked to evaluation the outputs (x.y), (x+y), and x' for these input signals.



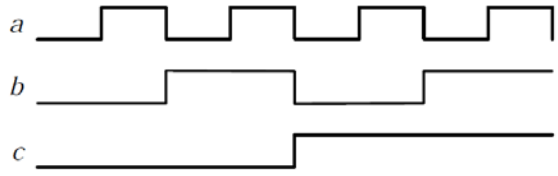
Example 2:

By means of a timing diagram, show the signal of the outputs f and g for the given circuit as a function of the three inputs a, b, and c. Use all possible combinations of a, b, c.

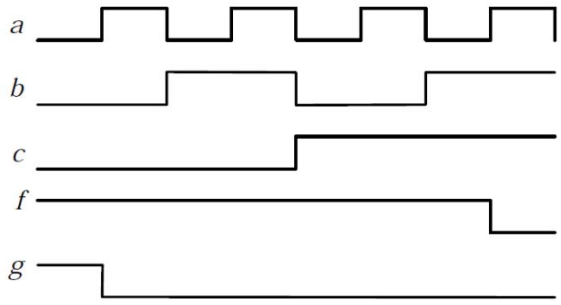


Solution:

Here we are NOT given the signals a, b, and c EXPLICITLY. The question is asking us to test for all combinations of a, b, and c (similar to a truth table). The input signals will look like this:

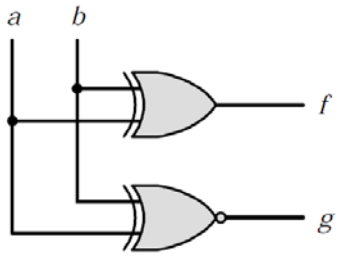


Note that a is the least significant variable while c is the most significant variable. Now we evaluate the outputs f and g as a function of these a, b, and c inputs as usual. The complete solution will look like:



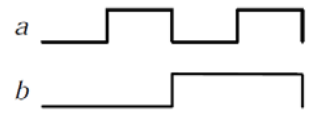
Example 3:

By means of a timing diagram, show the signals of the outputs f and g in the following circuit as a function of the two inputs a and b. Use four possible combinations of a and b.

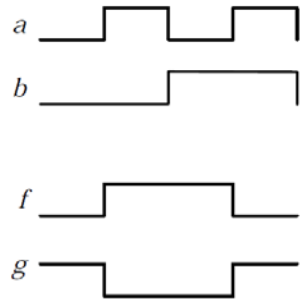


Solution:

Again, we are NOT given the signals a and b EXPLICITLY. The question is asking us to test for all combinations of a and b (similar to a truth table). The input signals will look like this:



Note that a is the least significant variable while b is the most significant variable. Now we evaluate the outputs f and g as a function of these a, b, and c inputs as usual. The complete solution will look like:



Note that the output of the XOR gate is 1 if the two inputs are different and 0 otherwise. The output of the XNOR gate is the opposite of the output of XOR gate.