KFUPM - ELECTRICAL ENGINEERING DEPARTMENT
EE-200 – Digital Logic Circuit Design (section 05) – Quiz07

Student Name:
Student Number:

### Problem (40 points):

It is desired to design a circuit that performs serial addition using two 4-bit shift registers (Shift register A and Shift register B). The partial circuit is provided in the figure below. Note that the external output Sum (*S*) is feedback to shift register A. The JK FF is used to store the carry produced by the addition of the two bits *x* and *y*.

a) Write the state table for the sequential circuit needed to perform the serial addition.

b) Derive the logic for variables J_Q, K_Q, and *S*, and Draw the logic circuit by completing the given figure.

c) Specify the steps needed to produce the sum of $N_1 = 1011$ and $N_2 = 0101$ and have it stored in shift register A. How many clock cycles are needed to perform this task?

d) Specify the contents of shift register A, shift register B, and the JF FF after performing the task in part (c).

Hint: The sequential circuit enclosed by the dashed rectangle has two inputs *x* and *y*, one state variable *Q*, and one external output *S*. Note that register A has NO external serial input!
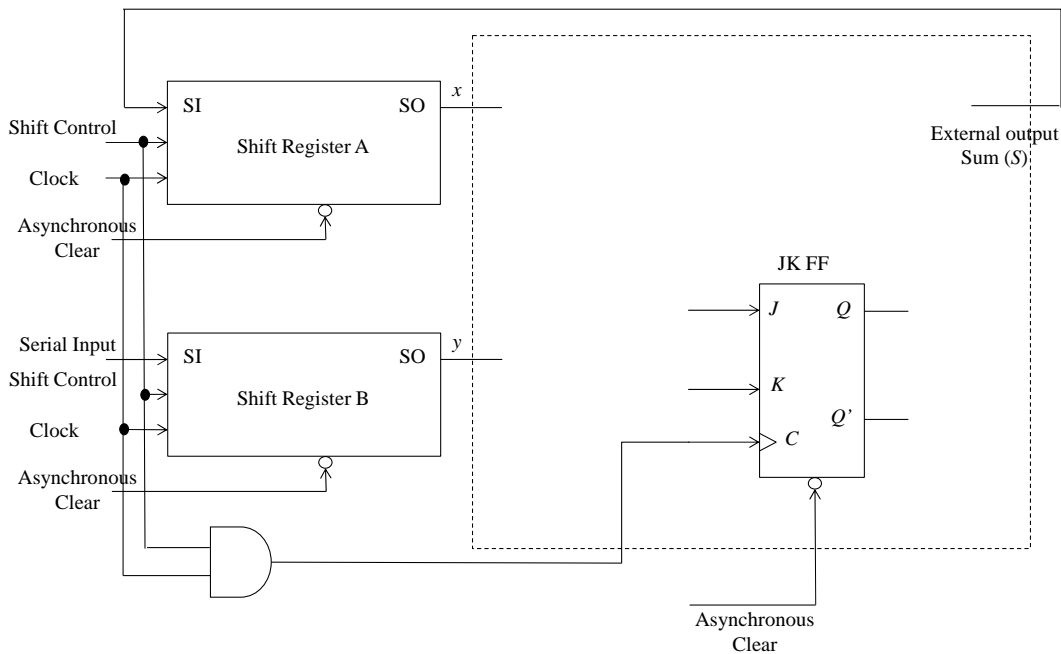
Serial adder (bit-by-bit addition using shift registers and a sequential circuit.