KFUPM - COMPUTER ENGINEERING DEPARTMENT
EE-200 – Digital Logic Circuit Design (section 05)
Assignment # 3: Due Sunday Nov 1st, 2015 – in class.

Problem	Points	Score
1	20	
2	30	
3	20	
4	20	
5	20	
6	30	
Total	140	

Problem 1 (20 points):
Simplify the following functions and implement them with two level NAND gate circuits:
a) $F(A, B, C, D) = (A' + C' + D')(A' + C')(C' + D')$
b) $F(A, B, C, D) = A' + AB + B'C + ACD$

Problem 2 (30 points):
Design a combinational circuit with 4 inputs and one output where the output is 1 when the binary value of the input is an even number. Implement the circuit using NAND only gates.
a) Derive the Boolean expressions for T1, T2, T3, and T4. Evaluate the outputs F1 and F2 as a function of the inputs A, B, C, and D.
b) Write the truth table for the functions F1 and F2 showing the intermediate variables T1, T2, T3, and T4.
c) Plot the output Boolean functions F1 and F2 from the truth table on maps and show that the simplified Boolean expressions are equivalent to the one obtained in part (a).
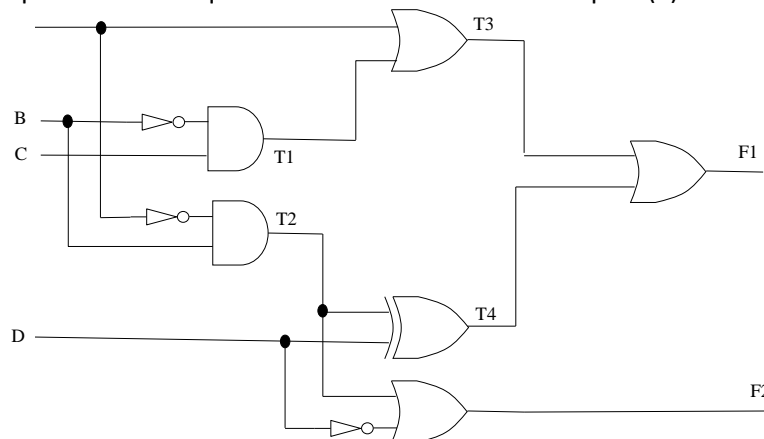

Figure P1. Circuit for Problem 1.

Problem 3 (20 points):
Design a combinational circuit with 4 inputs and one output where the output is 1 when the binary value of the input is an even number. Implement the circuit using NAND only gates.

Problem 4 (20 points):
Design a combinational circuit that computes the 9's complement of a BCD digit.

Problem 5 (20 points):
It is desired to design a BCD adder/subtractor circuit using the following blocks: (a) the BCD adder of Figure 4.14 of textbook, and (b) the 9's complement block of problem (4). Show the schematic diagram of your blocks and the relevant input and output lines of each block.

Problem 6 (30 points):
A full-subtractor circuit considers the inputs x, y, and B_{in}, where it subtracts the bit x from the bit y accounting the input borrow from the previous stage B_{in}. I.e. it performs the operation $y - x - B_{in}$ and produces the results $Diff$ and the output borrow B_{out}.
a) Design the full-subtractor block (using AND-OR implementation) and show a schematic diagram of the final block.
b) Draw the block diagram, use the block designed in part (a), for the circuit that may be used to subtract two 4-bit numbers.