KFUPM - COMPUTER ENGINEERING DEPARTMENT

EE-200 – Digital Logic Circuit Design (section 05)

Assignment # 2: Due Sunday Oct 4th, 2015 – in class.

Problem	Points	Score
1	50	
2	30	
3	30	
4	40	
Total	150	

Problem 1 (50 points):

Consider the circuit shown in Figure P1. The circuit has some specific implementation for the functions F1 and F2. The input variables are X, Y, and Z.

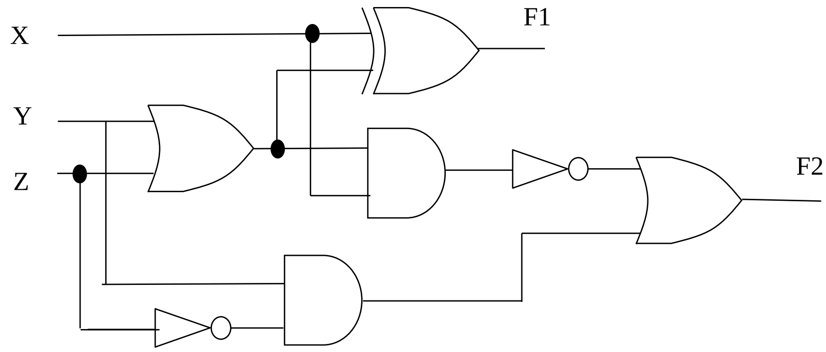

Figure P1. Circuit for Problem 1.

a) (4 points) Write the expressions for function F1 and F2 as implemented in by the circuit. i.e. without simplification.
b) (6 points) Using Boolean algebra simplify the expressions for F1 and F2 to the minimum number of literals.
c) (10 points) Use the expressions in part (a) to write the truth table for the two functions, then specify them as the sum of minterms.
d) (4 points) Write the function F1 as the product of maxterms.
e) (6 points) Use the simplified expression for F2 obtained in part (b) to obtain, using algebra, the sum of minterms form for F2.
f) (10 points) Use the simplified expression for F1 obtained in part (b) to obtain, using the algebra, the product of maxterms form for F1.
g) (10 points) Provide an AND-OR implementation for the functions F1 and F2.

Problem 2 (30 points):

Let F1(X, Y, Z) = X + Y'Z and F2(X, Y, Z) = ΠM(1, 2, 6, 7)
a) Express F1 in sum-of-minterms and product-of-maxterms.
b) Write F1.F2 (i.e. F1 ANDED with F2) as product-of-maxterms.
c) Express F1 + F2' in sum-of-minterms

Problem 3 (30 points):

Let F(A, B, C) = ΠM(1, 3, 6, 7)

a) (10 points) Minimize function F to a SOP expression with two terms each term is made of two literals. Simplify using Boolean algebra.
b) (8 points) Using minimum number of gates, implement function F using AND-OR implementation.
c) (12 points) Using minimum number of gates, implement function F using OR-AND implementation.

Problem 4 (40 points):

Let F(A, B, C) = AB’ + A’B + BC

Assume the variable and its complement are available

a) Implement F using AND, OR, and inverter gates

b) Implement F using OR and invert gates

c) Implement F using NAND and inverter gates

d) Implement F using NOR and inverter gates