King Fahd University of Petroleum and Minerals
Electrical Engineering Department

EE200: Digital Logic Circuit Design
Fall Semester 2015 (151)

A. Course Information

Text Book:	**Digital Design (5th Edition) by M. M. Mano**				
Course	Name		Office	Phone	Sections
Coordinator:	Dr. **Essam E. Hassan,** *ehassan@kfupm.edu.sa*		59/2100	2370	01, 02
Instructor:	Your Section Instructor is: **Dr Ashraf S. Mahmoud** *ashraf@kfupm.edu.sa* Office hours: UT 9:30-10:45 and 12:30-13:30 Or by appointment (email)		Bldg 22-420	1724	05 UTR 11:00-11:50 Rm 59-2025
Lab	Name		Office	Phone	Sections
Coordinator:	*Mr. Ahmad Fathi Saleem*				
Instructor:	Based on your section registration.				
Grading:	Assignments, and Quizzes	Laboratory	Attendance	Two Majors	Final
	17%	20%	3%	15% + 15%	30%
	1st Major	**2nd Major**	**Lab Final**	**Final**	
Exams Dates: **Exams Times:** **Exams Places:**	**October 13, 2015** 8 – 10 PM To be announced	**November 10, 2015** 6:30 – 8:30 PM To be announced	Your Lab time In your Lab	**December 26, 2015** 7:00 PM Register's website	
Important Dates:	Last day to drop the course without a permanent record	Last day to drop the course with "W" grade through the internet	**Last day of withdrawal from all courses with grade of "W" through the Registrar office**	Last day to drop all courses with "WP/WF" Thru Registrar's office.	
	September 3, 2015	October 8, 2015	November 5, 2015	December 3, 2015	

Note #1: All exams (**1st Major**, **2nd Major** and **Final Exam**) are **coordinated** (i.e. it is common for all sections). The Final Exam is **comprehensive** (covers chapters 1-6 as described in the syllabus and class notes). Lab Final will be given by the Lab instructor in the Lab during the normal Lab session.

Note #2: According to the rules and regulations of KFUPM, attendance is **MANDATORY**. More than **8** unexcused absences will be reported to the registrar office and result in a **GRADE of DN** regardless of the student's grade.

Note #3: It is your responsibility to solve the ***practice problems*** as soon as the material is covered in the class. Solution will be posted on **WebCT** (http://ocw.kfupm.edu.sa/). The ***practice problems*** set will not be collected.

Note #4: Your instructor may give you other home work assignments which will be collected and graded. Quizzes will be given regularly based on both the homework and the ***practice problems***...

Note #5: Class notes, announcements and HW solutions will be posted on the class webpage on WebCT **It is your responsibility to check announcements regularly.**

B. Course Details.

1. **Course (Catalog) Description**

   Number systems & codes. Logic gates. Boolean Algebra. Karnaugh maps. Analysis and synthesis of combinational systems, decoders, multiplexers, adders and subtractors, PLA's. Types of flip-flops. Memory concept. Registers. Introduction to sequential circuit design.

2. **Prerequisites(s)**

   Calculus I (MATH 101)
   General Physics I (PHYS 101)

3. **Course objectives** are to

   1. Introduce the students to the digital principles with emphasis on logic design.
   2. Familiarize the students with the necessary mathematical tools such as number systems, codes, and Boolean algebra.
   3. Learn the principles of analysis and design of combinational logic circuits
   4. Learn the principles of analysis and design of sequential logic circuits.

4. **Learning Outcomes**

   After successfully completing the course, the students will be able to

   Outcome1: apply knowledge of number systems, codes and Boolean algebra to the analysis and design of digital logic circuits.

   Outcome 2: identify, formulate, and solve engineering problems in the area of digital logic circuit design.

   Outcome 3: use the techniques, skills, and modern engineering tools such as logic works, necessary for engineering practice.

   Outcome 4: to function on multi-disciplinary teams through digital circuit experiments and projects.

   Outcome 5: to design a digital system, components or process to meet desired needs within realistic constraints.

5. **Topics Covered**

   - Binary Numbers, Number Base Conversions,
   - Complements, Signed Binary Numbers, Binary Codes,
   - Binary Logic, Boolean Algebra and digital logic gates,
   - Forms of logic functions and K-map simplification,
   - Analysis and design of combinational logic circuits,
   - Adders, Multipliers, Magnitude Comparator, Decoders, Multiplexers,
   - Programmable logic devices,
   - Flip-flops and sequential circuits,
   - Registers and counters.

6. **References.**
   - *Fundamentals of Digital Logic with Verilog Design*, S. Brown and Z. Vranesic, 2nd Edition, McGraw Hill, 2008.
   - *Logic and Computer Design Fundamentals*, M. Morris Mano and C. R. Kime, 4th Edition, Prentice Hall, 2008.

C. Tentative Course Outline and Schedule

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Week	Date	Topics	Sections	Labs/Prob. Sessions
1	Aug.23-27	Binary Numbers, Number Base Conversions,	1.1-1.3	No Lab
2	Aug.30-Sept.3	Octal & Hexadecimal Numbers, Complements, Signed Binary Numbers, Binary Codes	1.4-1.7	Exp. # 1
3	Sept.6-10	Binary Logic, Boolean Algebra: Axioms, Theorems & Properties. Boolean functions, Digital Logic Gates	1.9, 2.1-2.4 2.7-2.8	Exp. # 2
4	Sept. 13-17	Canonical & Standard Forms, More Logical Operations, Simplification of Boolean functions Using K-Maps, Product of Sums Simplification.	2.5-2.6 3.1-3.5	No lab
Eid AL-Adha Vacation				
5	Sept. 29-Oct. 1	Don't-care Conditions, NAND, NOR, and Other Two Level Implementations, Exclusive-OR Function.	3.6-3.9,3-10	No lab
6	Oct.4-8	Combinational Logic: Analysis and Design Procedures, Code Conversion, Adder circuits.	4.1-4.4	Exp. # 3
7	Oct. 11-15	Subtractors, Decimal Adder, binary multiplier, Magnitude Comparator, Decoders.	4.5-4.8	Exp. # 4
First Major Exam, Tuesday October 13, 2015. Time 8-10 pm				
8	Oct. 18-22	Encoders and Multiplexers	4.9-4.11,	Exp. # 5
9	Oct. 26-29	Sequential Circuits, Latches, Flip-flops, Characteristic Tables.	5.1-5.4	Exp. # 6
10	Nov. 1 -5	Analysis of Clocked Sequential Circuits, State Reduction and Assignment	5.5, 5.7	Exp. # 7
11	Nov. 8-12	. Flip-flop Excitation Tables, Design Procedure, Synthesis using different flip flops	5.8	Exp. # 8
Second Major Exam, Tuesday Nov. 10. Time 6:30-8:30 pm				
12	Nov. 15 - 19	Registers and Shift Registers.	6.1, 6.2	Exp. # 9
13	Nov. 22-26	Ripple Counters, Synchronous Counters and other counters	6.3-6.5	**Exp. # 10**
14	Nov. 29-Dec. 3	. , Random Access Memory, Programmable Logic, PLD'S, ROM, Programmable Logic Array, Programmable Array Logic	7-2,7-3, 7-5, 7-7	Final lab Projet
15	Dec. 6- 14	Revision		**Final Lab Exam.**

D. Practice Problems

Chapter 1: 3, 5, 9, 14, 18, 21, 23	Chapter 5: 2, 6, 7, 10, 12, 17, 18
Chapter 2: 2, 4, 9, 11, 15, 18, 22, 29	Chapter 6: 6, 8, 10, 16
Chapter 3: 7, 10, 15, 23, 26	Chapter 7: 6, 7, 8, 15, 19, 25
Chapter 4: 3, 5, 10, 11, 13, 21, 23, 25, 29	

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Week	Laboratory
1	No Lab.
2	Exp#1: Getting Started with the Laboratory Equipment
3	Exp#2: Building Logic Functions using Traditional ICs
4	No Lab.
5	No Lab.
6	Exp#3: Introduction to Verilog HDL and FPGA
7	Exp#4: Programming with Verilog HDL (Part I)
8	Exp#5: Programming with Verilog HDL (Part II)
9	Exp#6: Combinational Logic Circuits (Part I)
10	Exp#7: Combinational Logic Circuits (Part II)
11	Exp#8: Combinational Logic Circuits (Part III)
12	Exp#9: Sequential Logic Circuits (Part I)
13	Exp#10: Sequential Logic Circuits (Part II)
14	Exp#11: Final Lab Project
15	**Lab Final**

❖ Grade Policy

- Pre-labs 2
- Report 3
- Quizzes 4
- Project 4
- Final 7