King Fahd University of Petroleum & Minerals
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C314 اتصالات و شبكات الحاسب

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Lecture Contents

1. Asynchronous and Synchronous Transmission

Timing Requirement

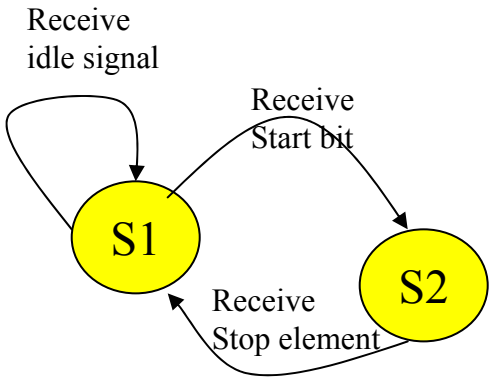
- Reception of digital data requires sampling of received signal at receiver → Sampling time should be known
- Clock drift (example):
  - If a receiver clock drifts by 1% every sample time,
  - Then for Tb = 1μsec, total drift after 50 bit times = 50 X 0.01 = 0.5 μsec
  - Hence, instead of sampling at the middle of the bit time, the receiver will sample at the edge of the bit (I.e. receiver is out-of-synch with transmitter clock)
- For correct reception, receiver clock/carrier should be synchronized with transmitter

Asynchronous Transmission

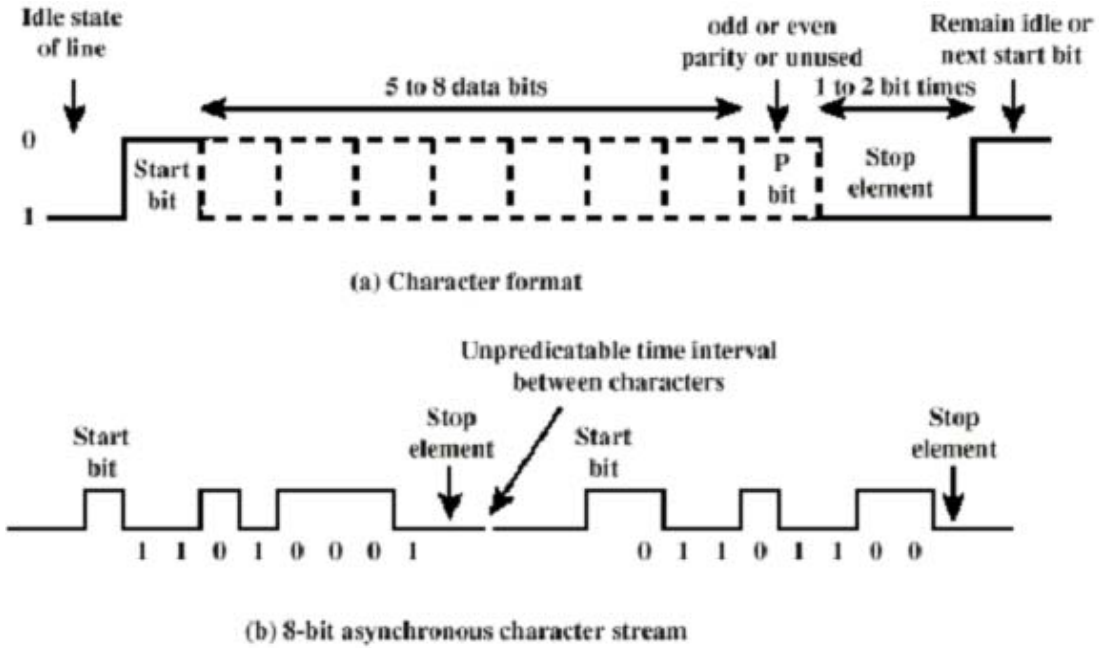
- Exploits: Rx-er can remain for short period in synch with Tx-er
- Used for short stream of bits – data transmitted one character (5 ~ 8 bits) at a time
- Synchronization is needed to be maintained for the length of short transmission
- Character is delimited (start & end) by known signal elements: start bit – stop element
- Rx-er re-synchs with the arrival of new character

Asynchronous Transmission

- Simple / Cheap
- Efficiency: transmit 1 start bit + 8 bit of data +2 stop bits ➔ Efficiency = 8/11 = 72% (or overhead = 3/11 = 28%)
- Good for data with large gaps (e.g. keyboard, etc)



S1: receiver in idle state
S2: receive is receiving character

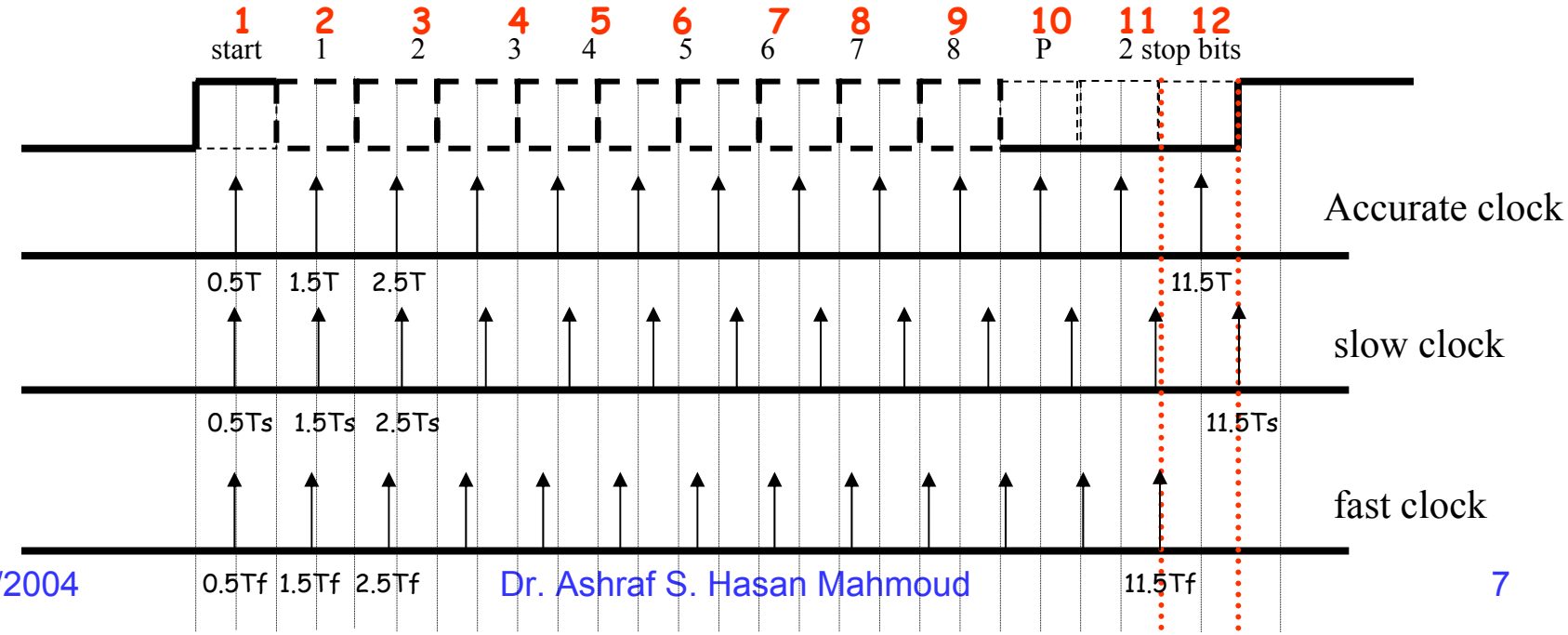


Example: Problem 6-5 Stallings

6-5: An asynchronous transmission scheme uses 8 bits, an even parity, and a stop element of length 2 bits. What percentage of clock inaccuracy can be tolerated at the receiver with respect to the framing error? Assume that the bit samples are taken at the middle of the clock period. Also assume that at the beginning of the start bit the clock and incoming bits are in phase.

Example: Problem 6-5- solution

- An accurate clock will start will start in phase (middle of first bit) and end end in phase (middle of last bit)
- However, a slow clock (time between two consecutive samples increases) will start in phase but will sample the last bit away from the middle of the actual bit duration – for this not to make a mistake it should sample <u>at most</u> at end of the last bit duration
- For a fast clock (time between two consecutive samples decreases) will start in phase but will sample the last bit before the middle of the actual bit duration – for this clock not to make a mistake it should sample <u>at least</u> at beginning of the last bit duration



Example: Problem 6-5 - solution (2)

Let the bit duration be T. Then a frame is 12T long.
Let a clock period be T'. The last bit (bit 12) is sampled at 11.5T'.

For a fast running clock, the condition to satisfy is

$$11.5T' > 11T \Rightarrow \frac{T}{T'} < \frac{11.5}{11} = 1.045 \Rightarrow f_{clock} < 1.045 f_{bit}$$

For a slow running clock, the condition to satisfy is

$$11.5T' < 12T \Rightarrow \frac{T}{T'} > \frac{11.5}{12} = 0.958 \Rightarrow f_{clock} > 0.958 f_{bit}$$

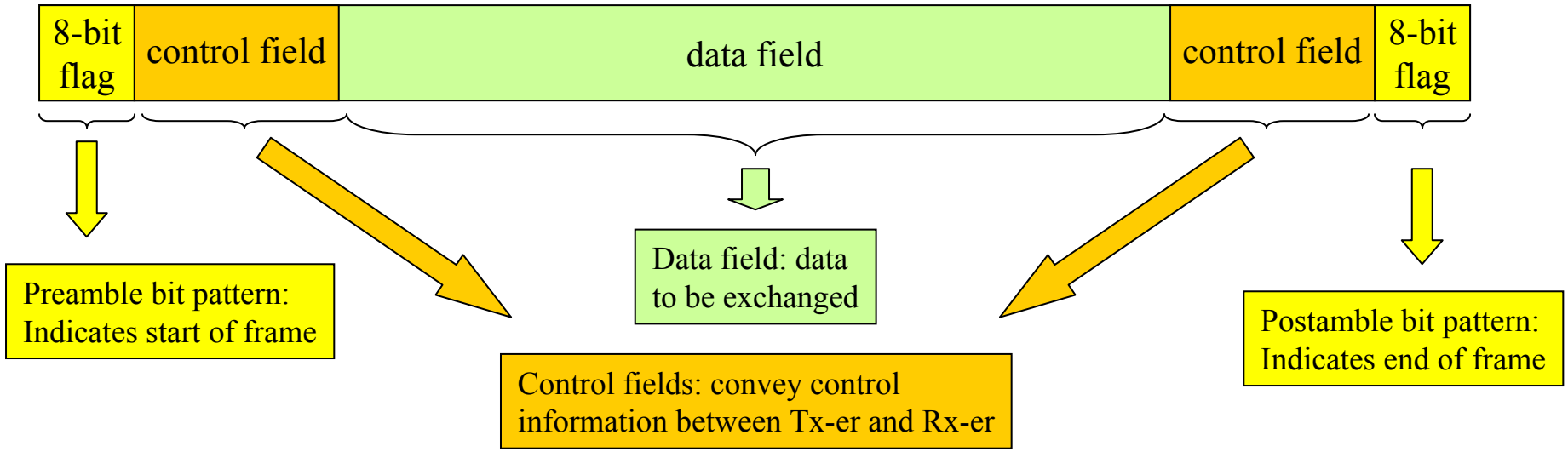
Therefore, the overall condition: 0.958 f_{bit} < f_{clock} <1.045 f_{bit}

Synchronous Transmission

- What if there is a STEADY STREAM of bits between Tx-er and Rx-er
  - Still use the start/stop bits ➔ low efficiency
  - Use synchronous transmission
- Synchronous Techniques:
  - Provide SEPARATE clock signal
    - Expensive and only good for short distances
  - Depend on data encoding to extract clock info
    - E.g. Manchester encoding

Synchronous Frame Format

- Typical Frame Structure



- For large data blocks, synchronous transmission is far more efficient than asynchronous:
  - E.g. HDLC frame (to be discussed in Chapter 7): 48 bits are used for control, preamble, and postamble – if 1000 bits are used for data ➔ efficiency = 99.4% (or overhead = 0.6%)