# KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

## COMPUTER ENGINEERING DEPARTMENT

## COE-202 – Fundamentals of Computer Engineering

**Assignment # 3: Due Tuesday January 27th, 2009 – in class.**

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**Problem 1: Implementation of BCD to 7-segment display controller**

It is desired to design and implement a BCD-to-7 segment display controller using the LogiSim tool. The BCD digit is represented by the bits ABCD where A is the MSB and D is the LSB. The design procedure is found in Lesson 3_1 page 6 of the online course notes. However, the 7-segment display component used in Lesson 3_1, shown in Fig. P1.1, has 7 input pins labeled c0, c1, …, and c6. Each one of the input pins is for one of the display segments. In LogiSim tool, the 7-segment display component has EIGHT input pins (4 pins from the top and 4 pins from the bottom). The 7-segment display component used in LogiSim is shown in Fig. P1.2. Before you proceed, you need to map 7 of the 8 input pins to the known labels c0, c1, …, and c6.

a) Implement the Kmaps and equations found on pages 7 and 8 of Lesson 3_1. This results in a combinational circuit whose inputs are A, B, C, and D, and has 7 outputs: c0, c1, …, c6. Save this circuit and call is a BCD-to-7-segment display controller.

b) Connect the circuit designed in (a) to the 7-segment display component in LogiSim.

You are required to test the operation of the BCD-to-7-segment display controller by applying various BCD inputs and observing the display on the 7-segments display component. Submit your circuit file electronically by email to rfarooqi@kfupm.edu.sa and to ashraf@kfupm.edu.sa, and also snap shots of the circuit in operation.

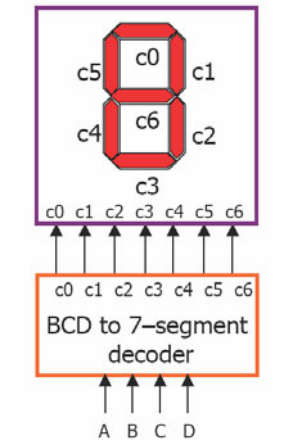


**Figure P1.1: 7-segment display using in Lesson 3_1 page 6.**

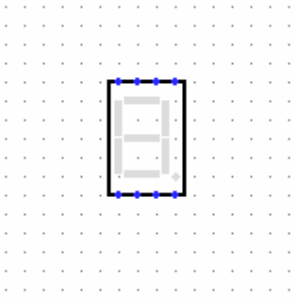

**Figure P1.2: 7-segment display component from LogiSim.**

**Problem 2: Design and Implementation of 4 bit Synchronous Binary Counter with Parallel Load**

It is desired to design a 4-bit synchronous binary counter with parallel load. The design of this counter is described in Lesson 5_3 of the online course notes. The overall design is also summarized in the slide from instructor notes shown below in Fig. P2.1. This counter circuit block designated by CTR-4 counts from 0000 to 1111 and back to 0000 again.

You are required to implement the circuit block CTR-4 and test its operation. Submit your circuit file electronically by email to rfarooqi@kfupm.edu.sa and to ashraf@kfupm.edu.sa, and also snap shots of the block in operation.

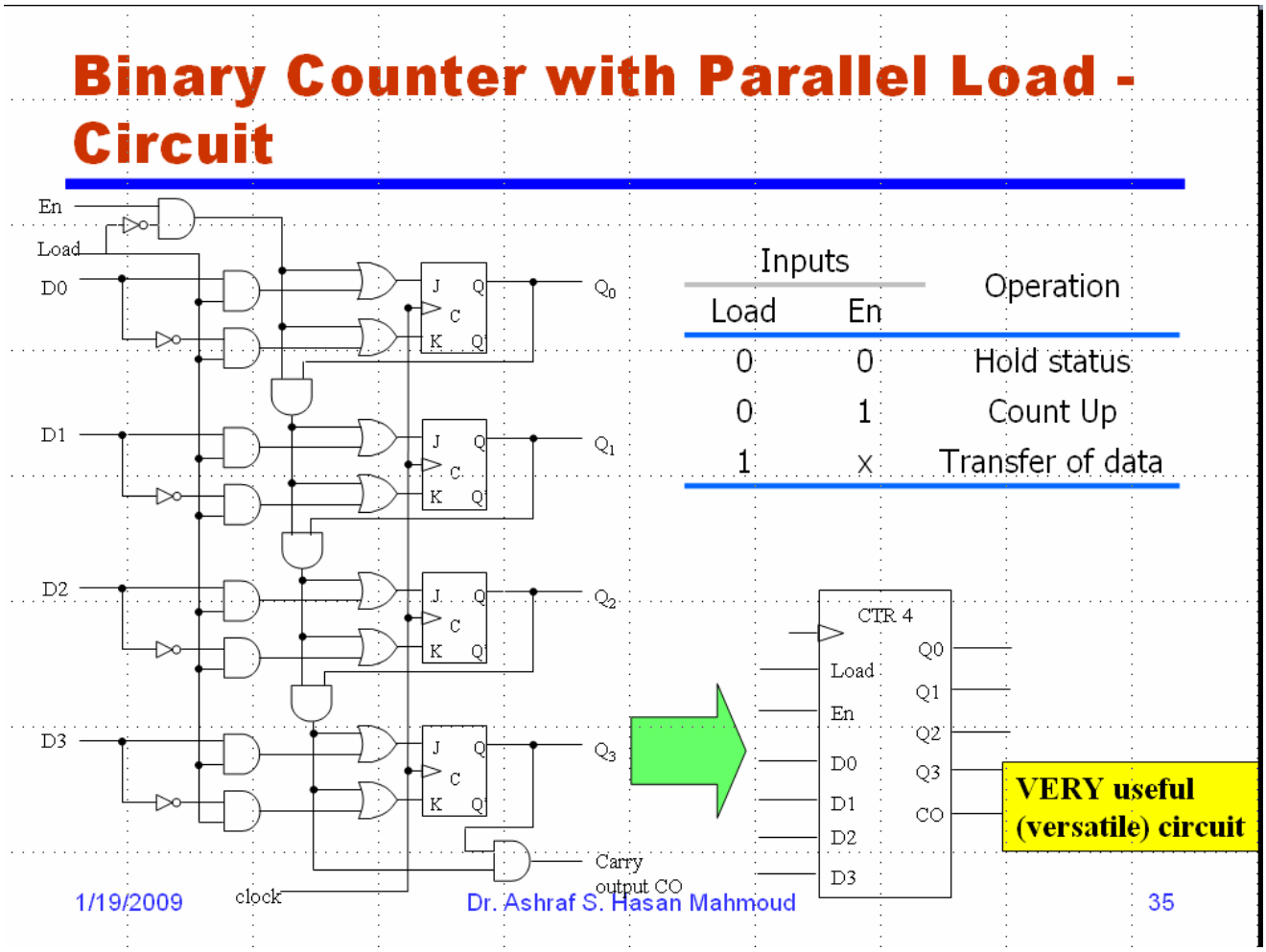


**Figure P2.1: Design of 4-bit SBC with parallel load.**

**Problem 3: Design and Implementation of BCD Counter**

It is desired to utilize the designs produced in problem 1 and problem 2 to design a BCD counter that counts from digit 0 to digit 9. The actual design procedure is sketched in Lesson 5_3 page 4 (Design of Decade counter). It is also found in the instructors power point notes slide 36.

Design the counter using the 4-bit SBC design in Problem 2. Connect the BCD-to-7 segment display to the counter output to display the generated count. You are required to test the circuit operation. Submit your circuit file electronically by email to rfarooqi@kfupm.edu.sa and to ashraf@kfupm.edu.sa, and also snap shots of the block in operation.