

KFUPM - COMPUTER ENGINEERING DEPARTMENT

COE-202 – Fundamentals of Computer Engineering

Assignment # 2: Due Sunday January 4th, 2008 – in class.

Problem 1) (20 points) Simplify the following Boolean functions to the form of sum-of-products by finding all prime implicants and essential prime implicants and applying the selection rule:

- a) $F(W,X,Y,Z) = \Sigma m(0,1,2,6,8,9,10,13)$
- b) $F(A,B,C,D) = \Pi M(1,3,5,6,7,9,10,11,14)$

Problem 2) (20 points) Simplify the following expressions in (1) sum-of-products and (2) product-of-sums forms. Use the K-map method for the simplification:

- a) $AC' + B'D + A'CD + ABCD$
- b) $(A' + B' + D)(A' + D')(A + B + D')(A + B' + C + D)$

Problem 3) (30 points) It is required to implement a 4-bit ripple carry adder using LogiSim:

- a) Implement the full adder circuit explained in class and shown in Figure P3a. Make this as an “FA” circuit added to your project.
- b) Add another circuit called “4-bit Ripple Carry Adder”. Use the FA block to construct the 4-bit carry adder. Test your new circuit with few examples and verify that it is performing the required function.

Provide screenshots for part (a) and part (b).

Hint: follow the instructions given in class and illustrated in <http://ozark.hendrix.edu/~burch/logisim/docs/2.1.0/guide/subcirc/using.html>

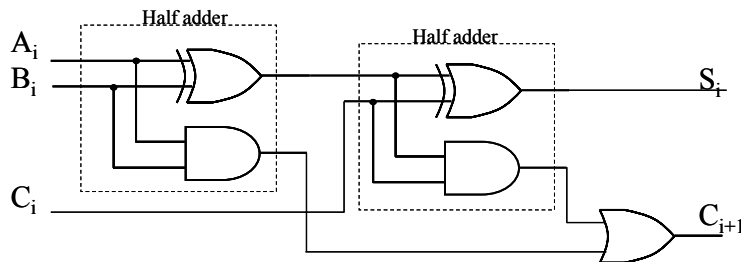


Figure P3a: Full adder circuit.

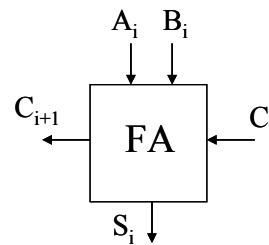


Figure P3b: Full adder block diagram.

Problem 4) (50 points) It is required to implement a 4-bit Carry Lookahead Adder (CLA) using LogiSim:

- a) Implement the partial adder circuit explained in class and shown in Figure P4a. Make this as a “PA” circuit added to your project.
- b) Add another circuit called “4-bit Carry Lookahead Adder”. Use the PA block to construct the 4-bit carry look ahead adder plus the required logic (AND and OR gates) to

generate the required carry signals. The construction procedure is as explained in class notes, and as shown in Figure P4c. Test your new circuit with few examples and verify that it is performing the required function.

Provide screenshots for part (a) and part (b).

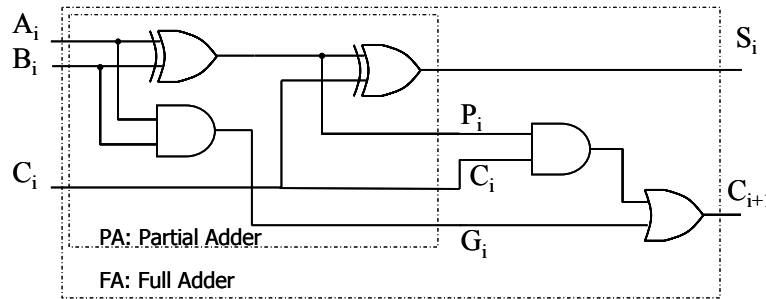


Figure 4a: Partial adder logic.

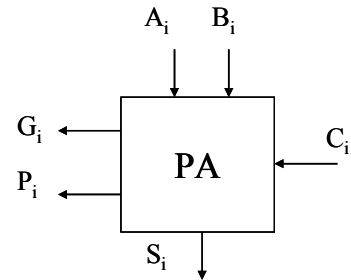


Figure 4a: Partial adder block.

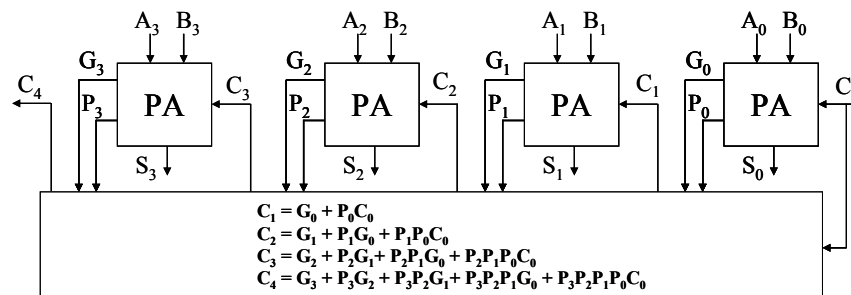


Figure 4c: Construction of 4-bit CLA.

Problem 5) (50 points) It is required to design a 4-bit ripple-borrow subtractor to find the subtraction $X - Y$ for the two unsigned numbers, $X = X_3 - X_0$, and $Y = Y_3 - Y_0$.

a) (25 points) Design a 1-bit full subtractor. The 1-bit full subtractor performs the following operation: $D = X - \text{bin} - Y$. Where D is the output, X , bin (borrow in), and Y are the input. Plot the truth table, and design the required circuit. Using a block diagram show how it can be used to construct the 4-bit ripple-borrow subtractor.

b) (25 points) Implement the 4-bit ripple-borrow subtractor in LogiSim and verify its operation. Provide several printouts displaying the required operation with selected examples of subtracting 4-bit numbers.

Problem 6) (50 points) Design a combinational circuit that receives a 4-bit signed number in 2's complement representation and returns the absolute value of the number i.e., the output returned should be 3-bit. Show all steps of design and implement your design in LogiSim. Submit several printouts displaying the function of your design.

Problem 7) (20 points) Construction of a 4-to-16 line decoder with enable input using five 2-to-4 line decoders with enable inputs. Do not use other logic gates.

Problem 8) (50 points) Construction of a 15-to-1 line multiplexer

a) Construct a 15-to-1 line multiplexer with two 8-to-1 line multiplexers. The corresponding figure depicts the multiplexer block and its functional table. Minimize the added logic required to have selection codes 0000 through 1110.

b) Use LogiSim to construct an 8-to-1 line multiplexer. Save the block under the name 8x1MUX. Use two of such blocks plus added logic gates to implement the final 15-to-1 line multiplexer using LogiSim. Submit both the designs for the 8-to-1 block and the 15-to-1 line multiplexer. Highlight on the submitted screen shots the operation of the 15-to-1 multiplexer

Hint: See the supplied figures: P8a, P8b, and P8c.

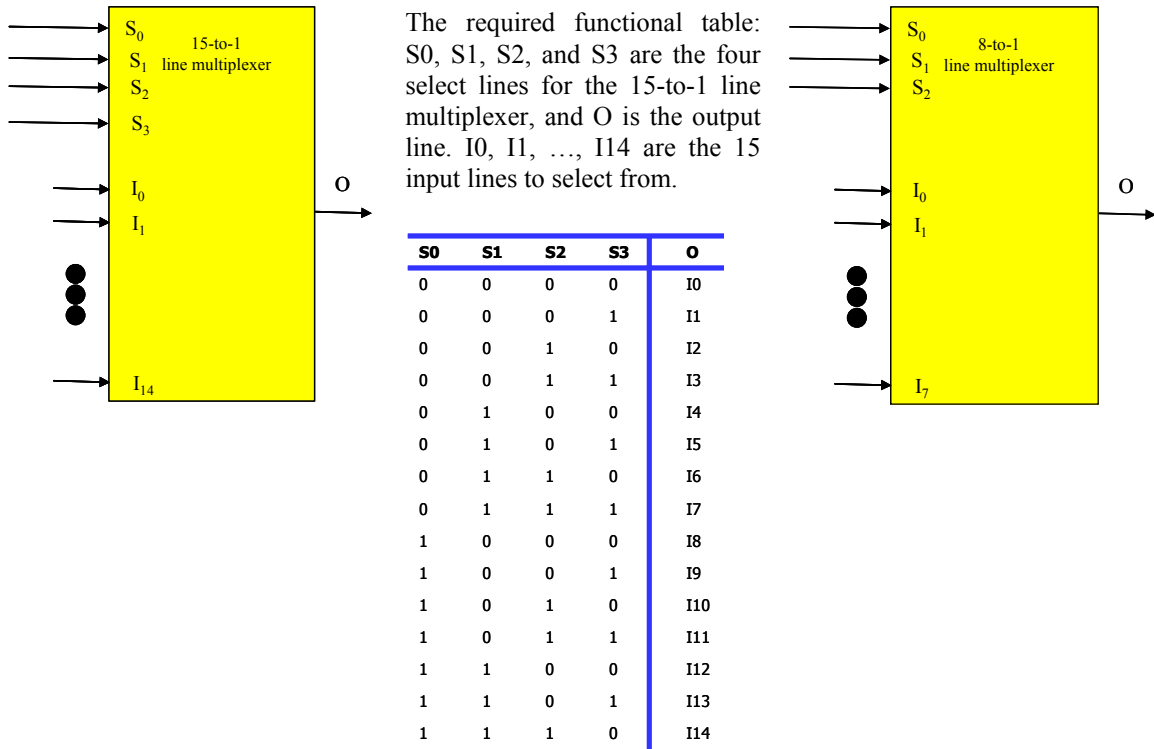


Figure P8a: 15-to-1 line multiplexer block.

Figure P8b: 15-to-1 line multiplexer functional table.

Figure P8c: 8-to-1 line multiplexer block.