

King Fahd University of Petroleum & Minerals Computer Engineering Dept

COE 341 – Data and Computer
Communications

Term 061

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Lecture Contents

1. Asynchronous and Synchronous Transmission
2. Error Detection
3. Error Correction (Optional)

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Timing Requirement

- Reception of digital data requires sampling of received signal at receiver → Sampling time should be known
- Clock drift (example):
 - If a receiver clock drifts by 1% every sample time,
 - Then for $T_b = 1\mu\text{sec}$, total drift after 50 bit times = $50 \times 0.01 = 0.5\mu\text{sec}$
 - Hence, instead of sampling at the middle of the bit time, the receiver will sample at the edge of the bit (I.e. receiver is out-of-synch with transmitter clock)
- For correct reception, receiver clock/carrier should be synchronized with transmitter

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Asynchronous Transmission

- Exploits: Rx-er can remain for short period in synch with Tx-er
- Used for short stream of bits – data transmitted one character (5 ~ 8 bits) at a time
- Synchronization is needed to be maintained for the length of short transmission
- Character is delimited (start & end) by known signal elements: start bit – stop element
- Rx-er re-synchs with the arrival of new character

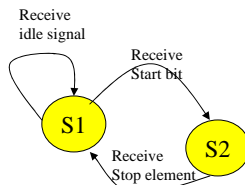
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Asynchronous Transmission

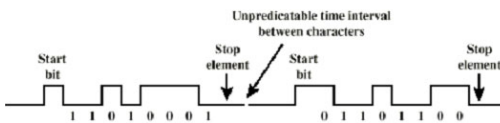
- Simple / Cheap
- Efficiency: transmit 1 start bit + 8 bit of data + 2 stop bits → Efficiency = $8/11 = 72\%$ (or overhead = $3/11 = 28\%$)
- Good for data with large gaps (e.g. keyboard, etc)



S1: receiver in idle state
S2: receiver is receiving character



(a) Character format



(b) 8-bit asynchronous character stream

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Example: Problem 6-5

6-5: An asynchronous transmission scheme uses 8 bits, an even parity, and a stop element of length 2 bits. What percentage of clock inaccuracy can be tolerated at the receiver with respect to the framing error? Assume that the bit samples are taken at the middle of the clock period. Also assume that at the beginning of the start bit the clock and incoming bits are in phase.

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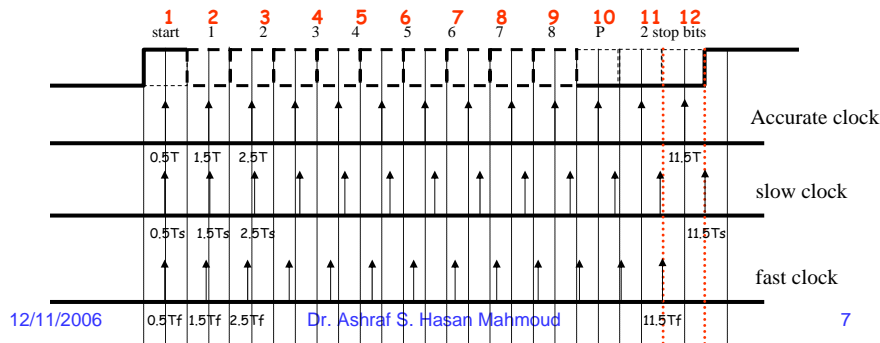
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Example: Problem 6-5- solution

An accurate clock will start in phase (middle of first bit) and end in phase (middle of last bit)

However, a slow clock (time between two consecutive samples increases) will start in phase but will sample the last bit away from the middle of the actual bit duration – for this not to make a mistake it should sample at most at end of the last bit duration

For a fast clock (time between two consecutive samples decreases) will start in phase but will sample the last bit before the middle of the actual bit duration – for this clock not to make a mistake it should sample at least at beginning of the last bit duration



Example: Problem 6-5 - solution (2)

Let the bit duration be T . Then a frame is $12T$ long.

Let a clock period be T' . The last bit (bit 12) is sampled at $11.5T'$.

For a fast running clock, the condition to satisfy is

$$11.5T' > 11T \Rightarrow \frac{T}{T'} < \frac{11.5}{11} = 1.045 \Rightarrow f_{clock} < 1.045 f_{bit}$$

For a slow running clock, the condition to satisfy is

$$11.5T' < 12T \Rightarrow \frac{T}{T'} > \frac{11.5}{12} = 0.958 \Rightarrow f_{clock} > 0.958 f_{bit}$$

Therefore, the overall condition: $0.958 f_{bit} < f_{clock} < 1.045 f_{bit}$

Synchronous Transmission

- What if there is a STEADY STREAM of bits between Tx-er and Rx-er
 - Still use the start/stop bits → low efficiency
 - Use synchronous transmission
- Synchronous Techniques:
 - Provide SEPARATE clock signal
 - Expensive and only good for short distances
 - Depend on data encoding to extract clock info
 - E.g. Manchester encoding

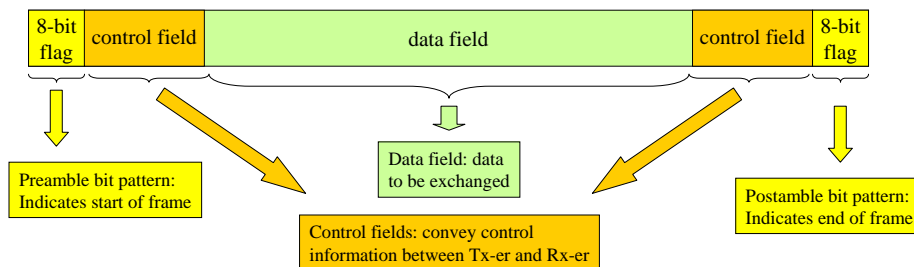
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Synchronous Frame Format

- Typical Frame Structure



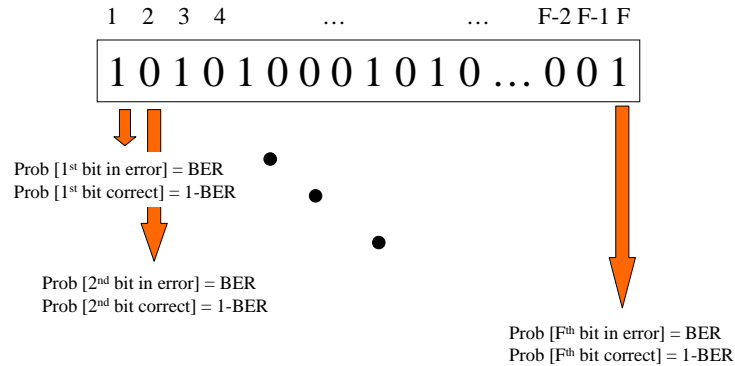
- For large data blocks, synchronous transmission is far more efficient than asynchronous:
 - E.g. HDLC frame (to be discussed in Chapter 7): 48 bits are used for control, preamble, and postamble – if 1000 bits are used for data → efficiency = 99.4% (or overhead = 0.6%)

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Error Detection



$$\text{Prob [k bits in error in frame]} = \binom{F}{k} (BER)^k (1 - BER)^{F-k}$$

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Error Detection – cont'd

- Hence, for a frame of F bits,

$$\begin{aligned} \text{Prob [frame is correct]} &= \text{Prob [0 bits in error]} \\ &= (1-BER)^F \end{aligned}$$

$$\begin{aligned} \text{Prob [frame is erroneous]} &= \text{Prob[1 OR MORE bits in error]} \\ &= 1 - \text{Prob[0 bits in error]} \\ &= 1 - (1-BER)^F \end{aligned}$$

Or

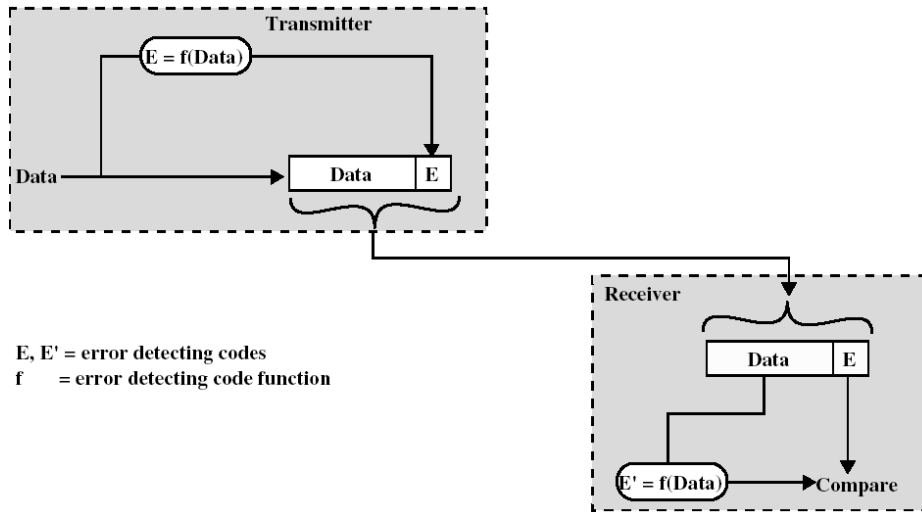
$$\begin{aligned} \text{Prob [frame is erroneous]} &= \text{Prob [1 bit in error]} + \\ &\quad \text{Prob[2 bits in error]} + \dots + \\ &\quad \text{Prob[F bits in error]} \\ &= 1 - \text{Prob[0 bits in error]} \\ &= 1 - (1-BER)^F \end{aligned}$$

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Error Detection (2)



E, E' = error detecting codes
 f = error detecting code function

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Cyclic Redundancy Check (CRC)



Processing: compute FCS (for some given an $n+1$ bit polynomial P)



$k+n$ bit frame to be transmitted = T

- Modulo 2 arithmetic (like XOR) is used to generate the FCS:
 - $0 \pm 0 = 0$; $1 \pm 0 = 1$; $0 \pm 1 = 1$; $1 \pm 1 = 0$
 - $1 \times 0 = 0$; $0 \times 1 = 0$; $1 \times 1 = 1$

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CRC – Mapping Binary Bits into Polynomials

- Consider the following k-bit word or frame and its polynomial equivalent:

$$b_{k-1} b_{k-2} \dots b_2 b_1 b_0 \rightarrow b_{k-1}x^{k-1} + b_{k-2}x^{k-2} + \dots + b_1x^1 + b_0$$

where b_i ($k-1 \leq i \leq 0$) is either 1 or 0

- Example1: an 8 bit word $M = 11011001$ is represented as $M(x) = x^7 + x^6 + x^4 + x^3 + 1$

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CRC – Mapping Binary Bits into Polynomials - cont'd

- Example2: What is $x^4M(x)$ equal to?

$x^4M(x) = x^4(x^7 + x^6 + x^4 + x^3 + 1) = x^{11} + x^{10} + x^8 + x^7 + x^4$, the equivalent bit pattern is 110110010000 (i.e. four zeros added to the left of the original M pattern)

- Example3: What is $x^4M(x) + (x^3 + x + 1)$?

$x^4M(x) + (x^3 + x + 1) = x^{11} + x^{10} + x^8 + x^7 + x^4 + x^3 + x + 1$, the equivalent bit pattern is 110110011011 (i.e. pattern 1011 = $x^3 + x + 1$ added to the left of the original M pattern)

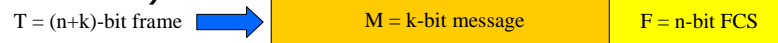
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CRC Calculation

- $T = (k+n)$ -bit frame to be tx-ed, $n < k$
- $M = k$ -bit message, the first k bits of frame T
- $F = n$ -bit FCS, the last n bits of frame T
- $P =$ pattern of $n+1$ bits (a predetermined divisor)



$P = (n+1)$ bit divisor

Note:

- $T(x)$ is the polynomial (of $k+n-1^{\text{st}}$ degree or less) representation of frame T
- $M(x)$ is the polynomial (of $k-1^{\text{st}}$ degree or less) representation of message M
- $F(x)$ is the polynomial (of $n-1^{\text{st}}$ degree or less) representation of FCS
- $P(x)$ is the polynomial (of n^{th} degree or less) representation of the divisor P
- $T(x) = X^n M(x) + F(x)$ – refer to example 3 on previous slide

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CRC Calculation (2)

- **Design:** frame T such that it divides the pattern P with no remainder?
- **Solution:** Since the first component of T , M , is the data part, it is required to find F (or the FCS) such that T divides P with no remainder

Using the polynomial equivalent:

$$T(x) = X^n M(x) + F(x)$$

One can show that $F(x) =$ remainder of $x^n M(x) / P(x)$

i.e if $x^n M(x) / P(x)$ is equal to $Q(x) + R(x)/P(x)$, then $F(x)$ is set to be equal to $R(x)$.

Note that:

Polynomial of degree $k+n$

----- = polynomial of degree k + remainder polynomial of degree $n-1$

Polynomial of degree n

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CRC Calculation - Procedure

1. Shift pattern M n bits to the left
2. Divide the new pattern $2^n M$ by the pattern P
3. The remainder of the division R (n bits) is set to be the FCS
4. The desired frame T is $2^n M$ plus the FCS bits

Note:

$2^n M$ is the pattern resulting from shifting the pattern M n bits to the left. In other words, the polynomial equivalent of the pattern $2^n M$ is $x^n M(x)$

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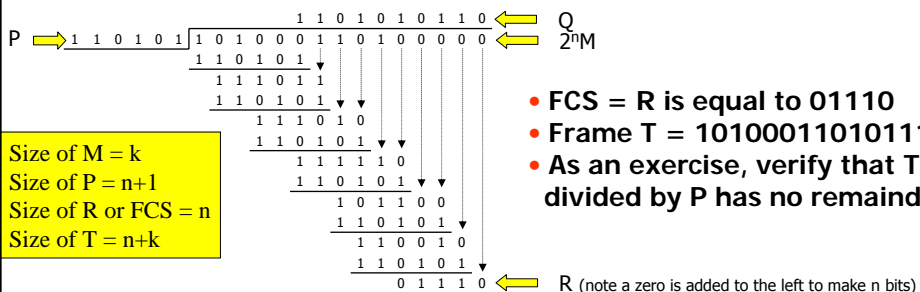
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CRC Calculation - Example

- Message M = 1010001101 (10 bits) $\rightarrow k = 10$
 Pattern P = 110101 (6 bits - note 0th and nth bits are 1s)
 $\rightarrow n + 1 = 6 \rightarrow n = 5$
 Find the frame T to be transmitted?

- Solution:



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CRC Calculation – The previous example BUT using Polynomials

- Message M = 1010001101 (10 bits) $\rightarrow k = 10$
- $M(x) = x^9 + x^7 + x^3 + x^2 + 1 \rightarrow x^5M(x) = x^{14} + x^{12} + x^8 + x^7 + x^5$
- Pattern P = 110101 (6 bits – note 0th and nth bits are 1) $\rightarrow n + 1 = 6 \rightarrow n = 5$
- $P(x) = x^5 + x^4 + x^2 + 1$
- Find the frame T to be transmitted?

Solution:

$$\begin{array}{r}
 \begin{array}{cccccccc}
 & x^9 & +x^8 & & +x^6 & & +x^4 & +x^2 & +x \\
 x^5 & +x^4 & +x^2 & +1 & & & & & \\
 \hline
 & x^{14} & & +x^{12} & & & +x^8 & +x^7 & +x^5 \\
 & x^{14} & +x^{13} & & +x^{11} & & +x^9 & & \\
 \hline
 & & x^{13} & +x^{12} & +x^{11} & & +x^9 & +x^8 & +x^7 & +x^5 \\
 & & x^{13} & +x^{12} & & & +x^{10} & +x^8 & & \\
 \hline
 & & & & x^{11} & +x^{10} & +x^9 & & +x^7 & +x^5 \\
 & & & & x^{11} & +x^{10} & & & +x^8 & +x^6 \\
 \hline
 & & & & & & x^9 & +x^8 & +x^7 & +x^6 & +x^5 \\
 & & & & & & x^9 & +x^8 & & +x^6 & +x^4 \\
 \hline
 & & & & & & & +x^7 & +x^5 & +x^4 \\
 & & & & & & & +x^7 & +x^6 & & +x^4 & +x^2 \\
 \hline
 & & & & & & & & x^6 & +x^5 & & +x^2 \\
 & & & & & & & & x^6 & +x^5 & & +x^3 & +x \\
 \hline
 & & & & & & & & & & & +x^3 & +x^2 & +x
 \end{array}
 \end{array}$$

- FCS = R(x) = x³ + x² + x
(or 0x⁴+x³+x²+x)
- R is equal to 01110
- Frame T = 101000110101110
- As an exercise, verify that T divided by P has no remainder

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CRC Calculation – The previous example BUT using Polynomials – cont'd

- Message M = 1010001101 (10 bits)
- $M(x) = x^9 + x^7 + x^3 + x^2 + 1$
- $x^5M(x) = x^{14} + x^{12} + x^8 + x^7 + x^5$
- Pattern P = 110101
- $P(x) = x^5 + x^4 + x^2 + 1$
- $R(x) = x^3 + x^2 + x$
- $Q(x) = x^9 + x^8 + x^6 + x^4 + x^2 + x$
- $T(x) = x^5M(x) + R(x)$
 $= x^{14} + x^{12} + x^8 + x^7 + x^5 + x^3 + x^2 + x$, or
T = 101000110101110
- Exercise: Verify that $Q(x)P(x) + R(x) = x^5M(x)$

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Example: Problem 6-12

6-12: for $P=110011$ and $M = 11100011$, find the CRC

```

                                     10110110
110011 / 1110001100000
         110011
         -----
          101111
          110011
          -----
           111000
           110011
           -----
            101100
            110011
            -----
             111110
             110011
             -----
              CRC = 11010
    
```

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CRC – Receiver Procedure

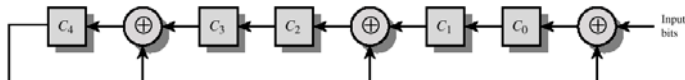
- Tx-er transmits frame T
- Channel introduces error pattern E
- Rx-er receives frame $T_r = T \oplus E$ (note that if $E = 000..000$, then T_r is equal to T , i.e. error free transmission)
- T_r is divided by P , Remainder of division is R
- if R is ZERO, Rx-er assumes no errors in frame; else Rx-er assumes erroneous frame
- If an error occurs and T_r is still divisible by $P \rightarrow$ **UNDETECTABLE** error (this means the E is also divisible by P)

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CRC – Transmitter Circuit



□ = 1-bit shift register ⊕ = Exclusive-OR circuit

(a) Shift-register implementation

Shift register circuit for dividing by
 $P = X^5 + X^4 + X^2 + 1$

	C_4	C_3	C_2	C_1	C_0	$C_4 \oplus C_3$	$C_4 \oplus C_1$	$C_4 \oplus \text{input}$	input
Initial	0	0	0	0	0	0	0	1	1
Step1	0	0	0	0	1	0	0	0	0
Step2	0	0	0	1	0	0	1	1	1
Step3	0	0	1	0	1	0	0	0	0
Step4	0	1	0	1	0	1	1	0	0
Step5	1	0	1	0	0	1	1	1	0
Step6	1	1	1	0	1	0	1	0	1
Step7	0	1	1	1	0	1	1	1	1
Step8	1	1	1	0	1	0	1	1	0
Step9	0	1	1	1	1	1	1	1	1
Step10	1	1	1	1	1	0	0	1	0
Step11	0	1	0	1	1	1	1	0	0
Step12	1	0	1	1	0	1	0	1	0
Step13	1	1	0	0	1	0	1	1	0
Step14	0	0	1	1	1	0	1	0	0
Step15	0	1	1	1	0	1	1	0	—

(b) Example with input of 1010001101

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CRC – Receiver Circuit

- Tx-er transmits frame T

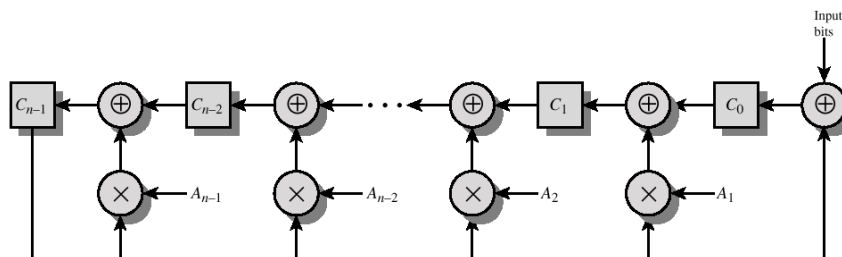


Figure 7.7 General CRC Architecture to Implement Divisor
 $1 + A_1X + A_2X^2 + \dots + A_{n-1}X^{n-1} + X^n$

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Cyclic Redundancy Check (CRC)

- Animation for [CRC Calculation](#)

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Example: Problem 6-13

A CRC is constructed to generate a 4-bit FCS for an 11-bit message. The generator polynomial is X^4+X^3+1

- Draw the shift register circuit that would perform this task (see figure 6.5)
- Encode the data bit sequence 10011011100 (leftmost bit is the LSB) using the generator polynomial and give the code word
- Now assume that bit 7 (counting from the LSB) in the code word is in error and show that the detection algorithm detects the error

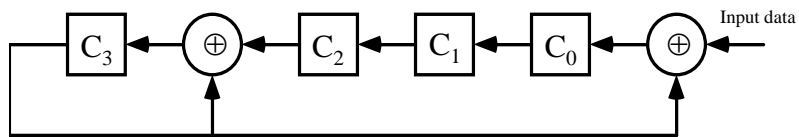
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Example: Problem 6-13 - solution

a)



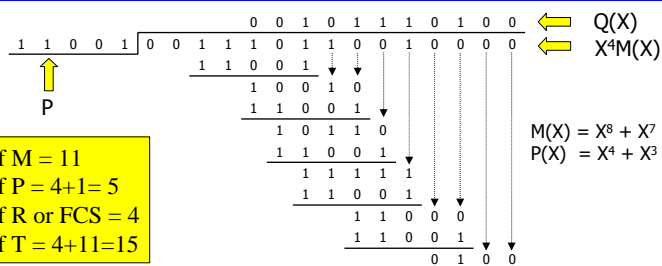
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Example: Problem 6-13 - solution

b)



Size of M = 11
 Size of P = 4+1= 5
 Size of R or FCS = 4
 Size of T = 4+11=15

$$M(X) = X^8 + X^7 + X^6 + X^4 + X^3 + 1$$

$$P(X) = X^4 + X^3 + 1$$

$$\rightarrow R = 0100 \text{ or } R(X) = X^2$$

Transmitted Frame T = 001110110010100

$$T(X) = X^4M(X) + R(X) = X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^4 + X^2$$

Notes:

1. $X^4M(X)/P(X) = Q(X) + R(X)/P(X)$, where $Q(X) = X^8 + X^6 + X^5 + X^4 + X^2$ (as seen from the long division process)
2. One can verify that $P(X)Q(X) + R(X)$ is indeed equal to $X^4M(X)$ {note that for the addition of polynomial terms modulo-2 applies; i.e. $X^9+X^9 = 0$ }

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Example: Problem 6-13 - solution

c) Received frame (LSB from the left) = 0 0 1 0 1 0 0 0 1 0 1 1 1 0 0
 dividing by P yields a nonzero remainder → error is detected
 Remainder = 0111

$$\begin{array}{r}
 \begin{array}{c} \text{↑} \\ \text{P} \end{array} \quad \begin{array}{r} \underline{1\ 1\ 0\ 0\ 1} \end{array} \bigg| \begin{array}{r} 0\ 0\ 1\ 1\ 1\ 0\ 1\ 0\ 0\ 0\ 1\ 0\ 1\ 1\ 1\ 0\ 0 \\ \underline{1\ 1\ 0\ 0\ 1} \\ 1\ 0\ 0\ 0\ 0 \\ \underline{1\ 1\ 0\ 0\ 1} \\ 1\ 0\ 0\ 1\ 0 \\ \underline{1\ 1\ 0\ 0\ 1} \\ 1\ 0\ 1\ 1\ 1 \\ \underline{1\ 1\ 0\ 0\ 1} \\ 1\ 1\ 1\ 0\ 0 \\ \underline{1\ 1\ 0\ 0\ 1} \\ 1\ 0\ 1\ 1\ 0 \\ \underline{1\ 1\ 0\ 0\ 1} \\ 1\ 1\ 1\ 1\ 0 \\ \underline{1\ 1\ 0\ 0\ 1} \\ 1\ 1\ 1 \end{array} \begin{array}{l} \leftarrow \text{RECEIVED FRAME} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \leftarrow \text{NON ZERO REMAINDER} \end{array}
 \end{array}$$

Textbook Problems of INTEREST

- Textbook Problems list: