

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

**COE 202 Fundamentals of Computer Engineering
Syllabus - Term 052**

Catalog Description

Introduction to Computer Engineering. Digital Circuits. Boolean algebra and switching theory. Manipulation and minimization of Boolean functions. Combinational circuits analysis and design, multiplexers, decoders and adders. Sequential circuit analysis and design, basic flip-flops, clocking and edge-triggering, registers, counters, timing sequences, state assignment and reduction techniques. Register transfer level operations. (*Prerequisite: PHYS 102*)

Instructor

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Class

Time 11:00- 12:15

SM

Location

Room 22-119

Office Hours: Sat/Mon 09:00-11:00 am, and by appointment.

Text Book: Morris Mano and Charles Kime, *Logic and Computer Design Fundamentals*, Second Edition, Prentice Hall International, 2000.

Grading Policy:	Class work & Quizzes	20%
	Exam I	20%
	Exam II	25%
	Final	35%
	Total	100% (PLUS bonus for perfect attendance and active participation)

Course Topics

Week	Class #	Subject	Ref
Number System and Codes			
1	1.	Introduction. Information Processing, and representation. Digital vs Analog	1.1
	2.	Number Systems. Binary, octal and hexadecimal numbers	1.2, 1.3
2	3.	Number base conversion (Dec to Bin, Oct, and Hex, General)	1.3
	4.	Conv (Bin, OCT, Hex), Binary & other System Arith.	1.3
	5.	Signed Binary Number representation, Signed Mag, R's &(R-1)'s Complement	Handout
3	6.	Signed Binary Addition and Subtraction. R's &(R-1)'s Complement	Handout

	7.	Signed Binary Addition and Subtraction. R's &(R-1)'s Complement	Handout
	8.	Codes. BCD, Excess-3, Parity Bits, ASCII & Uni-Codes	1.4, 1.5, Handout

Binary Logic & Gates			
4	9.	Binary logic and gates, Boolean Algebra, Basic identities of Boolean algebra.	2.1, 2.2
	10.	Boolean functions, Algebraic manipulation, Complement of a function.	2.2
	11.	Canonical and Standard forms, Minterms and Maxterms, Sum of products and Products of Sums.	2.3
5	12.	<i>Map method of simplification:</i> Two-, Three-, and Four-variable K-Map.	2.4
	13.	<i>Map method of simplification:</i> Five, and Six-variable K-Map.	Handout
6	14.	<i>Map manipulation:</i> Essential prime implicants, Nonessential prime implicants, Simplification procedure.	2.4
	15.	Don't care conditions and Simplification	2.5
	16.	Universal gates; <i>NAND and NOR gates:</i> 2-level implementation.	2.6
7	17.	<i>Multilevel NAND Circuits.</i>	2.6
	18.	Exclusive-OR (XOR) and Equivalence (XNOR) gates, Parity generation and checking.	2.7
Combinational Logic			
	19.	Combinational Logic, Design procedure. BCD-to-Excess 3 code Conversion.	3.4
8	20.	BCD-to- 7 Seg. Display. Half and Full Adders.	Partial 3.4, 3.8
	21.	Design using MSI parts. Decoders, Decoder Expansion. Combinational Circuit implementation using decoders.	3.5
	22.	Encoders & Priority Encoders <i>Magnitude Comparator.</i>	3.6, Handout
9	23.	Multiplexers. Function Implementation using multiplexers, Demultiplexers	3.7
	24.	<i>Binary Adders: 4-Bit Ripple Carry Adder, Carry Look-Ahead Adder, Binary Adder-Subtractor.</i>	3.8, 3.10
	25.	BCD Adder, Binary Multiplier.	3.11, 3.12
Sequential Circuits			
10	26.	<i>Sequential Circuits:</i> Latches, SR and D-latch, Clocked latch.	4.1, 4.2
	27.	<i>Flip-Flops:</i> Master-Slave, Edge-Triggered. <i>Timing Diagrams</i>	4.3
11	28.	<i>Flip-Flops Characteristic & Excitation Tables:</i> D-FF, SR-FF, JK-FF, T-FF.. <i>Asynchronous/Direct Clear and Set Inputs</i>	4.3
	29.	Setup, Hold, Enable times. Timing control and Clocks. Path delay constraints.	Handout
	30.	<i>Sequential Circuit Design:</i> Design procedure, Construction of state diagrams and state tables.	4.5
12	31.	Designing with D-FFs. Designing with unused states.	4.6
	32.	Designing with JK-FFs, Flip-Flop	4.7
	33.	Sequential Circuit Design Examples.	
13	34.	<i>Sequential Circuit Analysis:</i> Input equations, State table.	4.4

Registers & Counters			
	35.	Registers, Registers with parallel load, Shift Registers.	5.2, 5.3
	36.	Shift register with parallel load, Bi-directional shift register.	5.3
14	37.	<i>Ripple Counters:</i> Up-Down Counters. Synchronous Binary Counters: <i>Counters with JK-FF, Counters with D-FF.</i>	5.4
	38.	<i>Serial and Parallel Counter, Up-Down Binary Counter, Binary Counter with Parallel Load.</i>	<u>5.5</u>
	39.	Other Counters: BCD Counter, Arbitrary Count Sequence.	5.5
Memory & PLDs			
15	40.	<i>Memory and Programmable Logic Devices:</i> Read-Only Memory.	6.1, 6.7
	41.	Combinational Circuit Implementation with ROM.	6.7
	42.	Programmable logic Array, Programmable Array logic. Programmable Logic Devices and FPGAs	6.8, 6.9