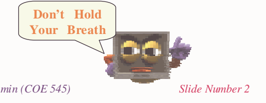
DIGITAL SYSTEM TESTING
COE -545

Lecture - 02

Feasibility of Exhaustive Testing

Example

- Consider a *Small-Size IC* of 20 PI`s and 100 FFs. Assuming a testing frequency of 1GHz, Estimate the time required to Exhaustively Test this device.
- The Minimum # of Test Patterns= $2^{(20+100)}=2^{120}$
- Time taken by Each Test Pattern = $1/10^9$ = 1 Nano-Second
- Lower Bound on the Required Test Time= $10^{-9} \times 2^{120}$ = 42,120,693,455,298,117,502 years ≈ 42×10^{18} years



Alternative to Exhaustive Testing

- Functional Tests: *Validates, in a Cost-Effective Way, If a Given CKT Performs its intended Function*
  - *Test Stimuli Are Applied at a Relaxed Frequency (Much Slower Than Normal Speed) To Avoid AC Speed Sensitivities.*
- Exhaustive Functional Testing is a *Computationally Intractable* Problem (only feasible for very small CUTs) → Cannot Fully Verify All Circuit States → *Not Cost-Effective*
- **Instead** of Exhaustive Testing for Proper Operation, *We Test for the ABSENCE of Faults from the circuit.*
- The List of Possible Faults (***Fault List***) Must be of a *Manageable Finite Size*

Physical Faults (Defects)

- The Number of ALL Possible *Physical Faults* (Defects) in any Product is ***HUGE***
- Huge Fault List Based on *Physical Faults* (Defects) → *Computationally Intractable*
- Physical Faults (Defects) Can Be Introduced During Any Fabrication Step.

Physical Faults (Defects)

Example for a VLSI Chip:

- Material Defects →
  - Bulk defects (cracks, crystal imperfections)
  - Surface impurities (ion migration)
  - Passivation pits and cracks
  - Gate oxide Defects → breakdown
    - Pinholes or thin spots in oxide
    - Electrical over-stress
  - Surface potential instability → Threshold Voltage Instability
- Photolithographic & Fabrication Errors →
  - Missing Contact Woindows
  - Signal Shorts (Metal Bridging, Pinholes),
  - Signal Open (Defects, Metal Step Coverage)

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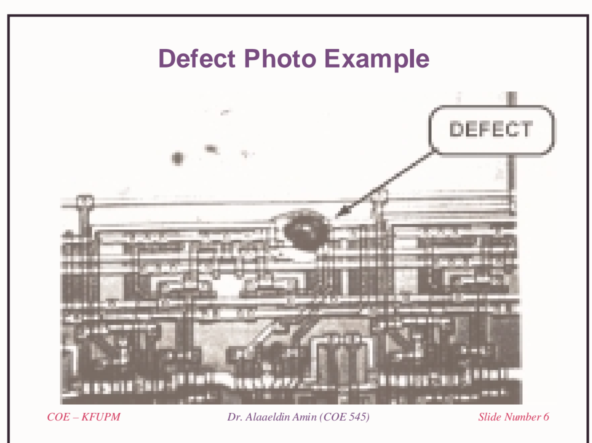

Defect Photo Example

- Packaging Defects
  - Contact Defect (Wire Bonding Failure)
  - Improper Die-Attach
  - Improper Sealing
- Wear out Defects
  - Electromigration
  - Oxide Charges & VT Shifts (Hot Carrier Effects)
  - Dielectric Breakdown
- Environmental Effects
  - Radiation Effects, ALPHA Particles, Temperature, etc.

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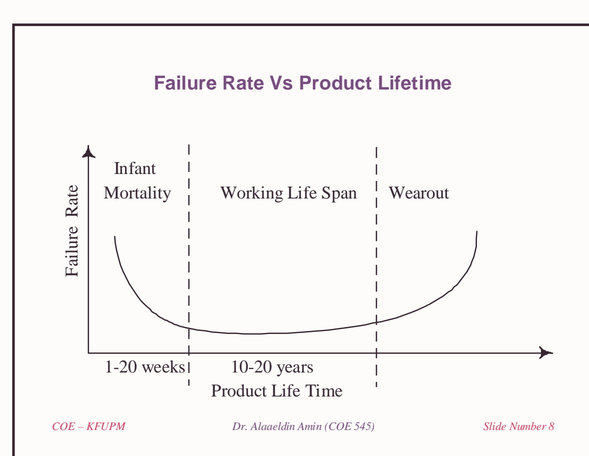
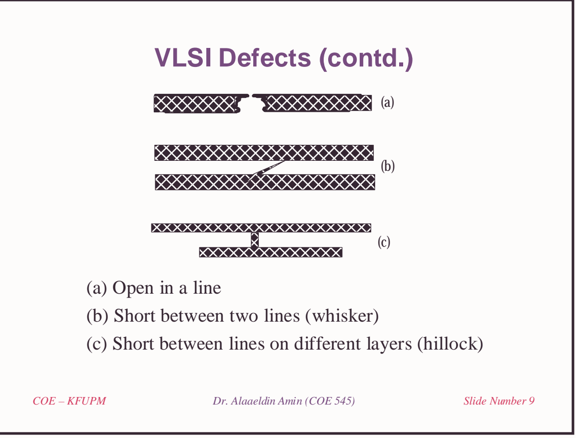


VLSI Defects (contd.)



(a) Open in a line
(b) Short between two lines (whisker)
(c) Short between lines on different layers (hillock)

Observed PCB Defects

Defect classes	Occurrence frequency (%)
Shorts	51
Opens	1
Missing components	6
Wrong components	13
Reversed components	6
Bent leads	8
Analog specifications	5
Digital logic	5
Performance (timing)	5

Ref.: J. Bateson, *In-Circuit Testing*, Van Nostrand Reinhold, 1985.

Conclusions?

- Exhaustive Functional Testing is a *Computationally Intractable* For Most Systems.
- *Testing for the **ABSENCE** of Faults Requires* a ***Fault List*** of *Manageable Size*
- *Physical Faults* (Defects) too Numerous and Often not Easily Analyzable to form a Useful Fault List.
- Instead, a ***Logical Fault Model*** Needs To Be Adopted.

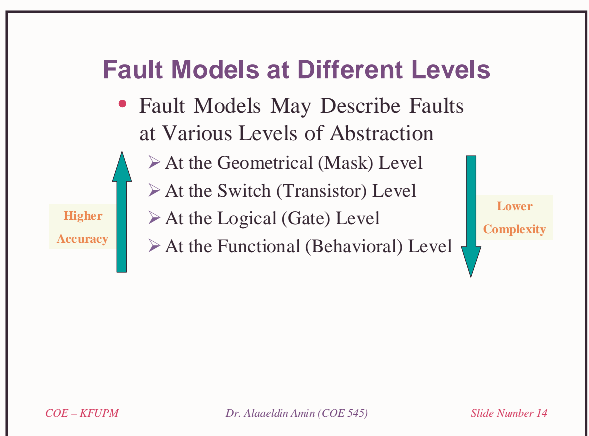
Why Fault Models?

- Models are often easier to work with, e.g. one logical fault can cover many physical ones (defects).
- Models are portable
- Models can be used for simulation, thus avoiding expensive hardware/actual circuit implementation
- Nearly all engineering systems are studied using models
- All the above apply for logic as well as for fault modeling

Fault Model Requirements

1. Accuracy.
   - The Logical Model Should Represent the Circuit Behavior Under Realistic Physical Fault Condition.
2. Tractability (*Cost-Effectiveness*).
   - The Logical Fault Model Should Have a Manageable Complexity, both for Test Generation and Test Application.

- Engineering Tradeoff is Involved in the Choice of a Fault Model. The more Accurate the Model IS the More Complex (and Less Tractable) it will be.



Types of Logical Fault Models

1. Structural Fault Models.
   - Defined in Conjunction with a Circuit Structure
   - Their Effect is to Modify Interconnection between Components while Components themselves are Assumed to Be Fault Free (e.g. Stuck_at, Bridging, and Transistor-Level Fault Models)
   - Not Possible if Detailed Structural Description is Not Available
   - More Structural Details Increases the Complexity of Test Generation
2. Functional Fault Models.
   - Defined in Conjunction with a Functional Model, independent of a Specific Implementation
   - Their Effect is to Change the Function of Components Without Worrying about their Interconnection
   - Examples Include Changes in a Truth Table of a Component Cross Point Faults in PLAs, Pattern-Sensitive Faults in RAMs, etc.
   - Useful when Detailed Structural Description is Not Available

W.R.T. Time , Physical Faults Can Be Classified As:-

1. **Transient Faults**
   - Temporary, Non-Recurring Faults, e.g. Due to Power Supply Fluctuations and Alpha-Particle Induced Faults
2. **Intermittent Faults**
   - Recurring Faults that Appear Under a Given Set of Circumstances Due to Some Unstable Physical Condition
   - Generally May Result From
     - Poor Design
     - Partially Defective Elements
     - Loose Interconnects
     - Ambient Conditions

Too Difficult To Model

W.R.T. Time , Physical Faults Can Be Classified As:-

3. **Permanent Faults**
   - This is the Category of Faults that We Will Consider.

W.R.T. # of Faults , Fault Models Are Classified As:

1. **Single Fault Model**
   - Only One Fault Existes at a Time. More Commonly Used Since It is
     - Less Complex
     - Covers (Detects) Most Multiple Faults
2. **Multiple Fault Model**
   - More Than one Fault May Exist at a Time

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Fault Effects

- On the electrical level
  - Most physical defects results into
    - Opens
    - Shorts
- Effect of open:
  - technology dependent (*e.g. TTL I/P → Logic 1, Transistor Open → Sequential Behavior*)
  - not strictly high-Z behavior (*e.g. TTL I/P*)
- Effect of a Short:
  - Solid Short (*0 Resistance*) Usually Assumed
  - Realistically Finite Resistance

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Common Fault Models

Fault Model	Description
Single Stuck-at Faults (SSA)	One line (Signal) gets Stuck at a constant value either a 0 or 1.
Multiple Stuck-at Faults	Two or more lines have fixed values, not necessarily the same.
Bridging Faults	Two or more lines that are normally independent get shorted together.

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More Fault Types

Fault Model	Description
Stuck-Open Faults (SOP)	A failure in a pull-up or pull-down transistor in a CMOS logic causes it to behave as a memory element
Stuck-On Faults (SON)	A transistor is always conducting.
Delay Faults	A fault is caused by delays in one or more Gate/path in the circuit.
Pattern Sensitive Faults	Fault Model for Memory Arrays where data stored in some Cell(s) are affected by the stored Data Pattern in Neighboring Cells

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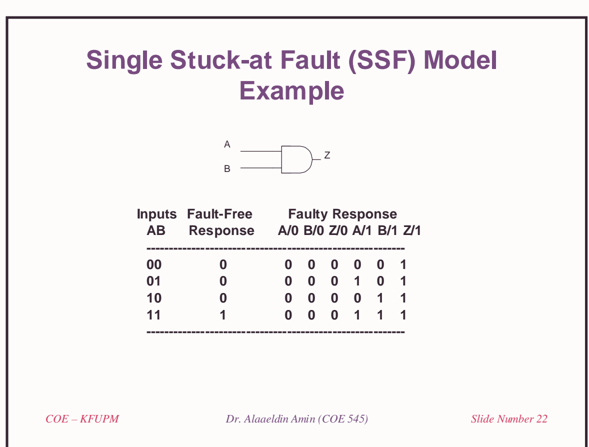
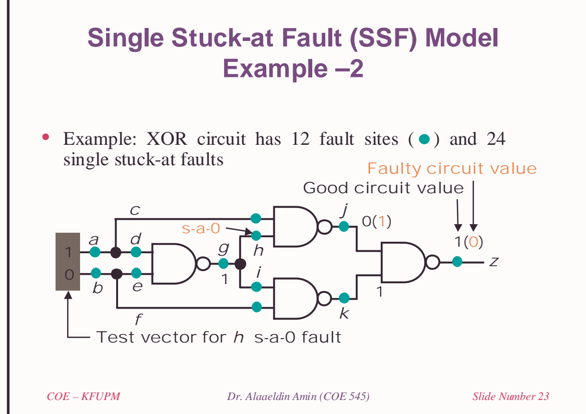
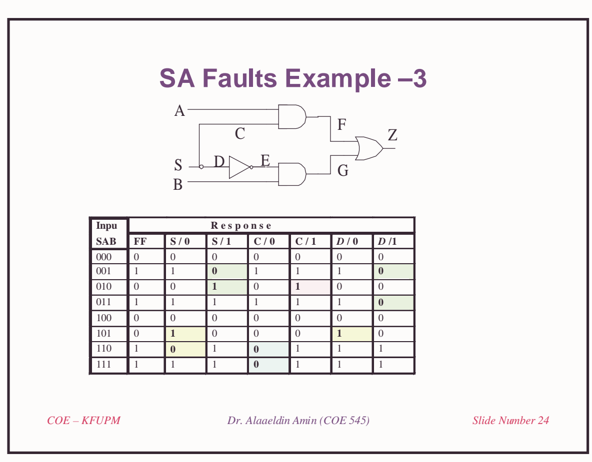
Single Stuck-at Fault (SSF) Model

- Three properties Characterize a Single-Stuck-at Fault (SSF)
  - Only one line is faulty
  - Faulty line has a Fixed 0 or 1 Value Independent of Other Signal Values
  - The fault can be at an input or output of a gate
- It is Technology-Independent.
- Experience shows that tests covering SSFs are Highly Likely to Detect Many Other Types of Non-Classical Faults.
- Many (But not All) Physical Faults (Defects Can be Represented by this Model.
- If Signal *x* is Stuck at value *i*, we Write ***x / I***
- *Every Line **L** Has 2 Possible Faults* (***L / 0***), **and** (***L / 1***)

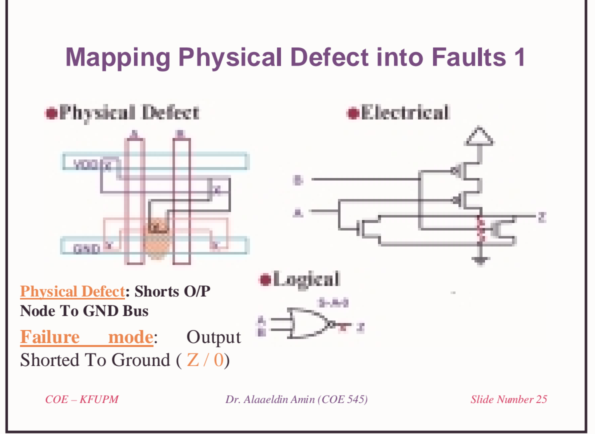


Inputs AB	Fault-Free Response	Faulty Response A/0	B/0	Z/0	A/1	B/1	Z/1
00	0	0	0	0	0	0	1
01	0	0	0	0	1	0	1
10	0	0	0	0	0	1	1
11	1	0	0	0	1	1	1





Inpu SAB	Response FF	S / 0	S / 1	C / 0	C / 1	D / 0	D /1
000	0	0	0	0	0	0	0
001	1	1	**0**	1	1	1	**0**
010	0	0	**1**	0	**1**	0	0
011	1	1	1	1	1	1	**0**
100	0	0	0	0	0	0	0
101	0	**1**	0	0	0	**1**	0
110	1	**0**	1	**0**	1	1	1
111	1	1	1	**0**	1	1	1


Mapping Physical Defect into Faults 1
Physical Defect
Electrical
Logical
Physical Defect: Shorts O/P Node To GND Bus
Failure mode: Output Shorted To Ground (Z / 0)
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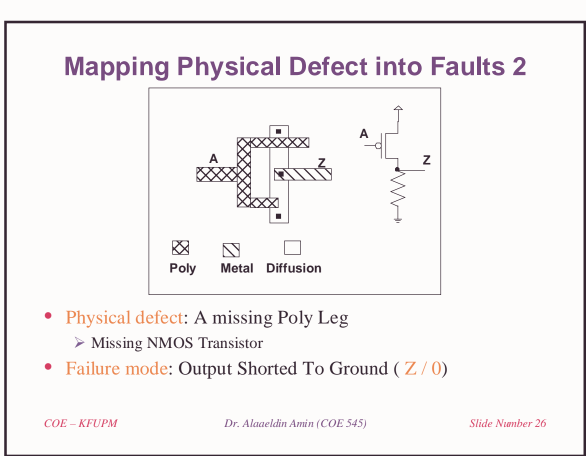
Mapping Physical Defect into Faults 2
A
Z
Poly
Metal
Diffusion
Physical defect: A missing Poly Leg
Missing NMOS Transistor
Failure mode: Output Shorted To Ground (Z / 0)
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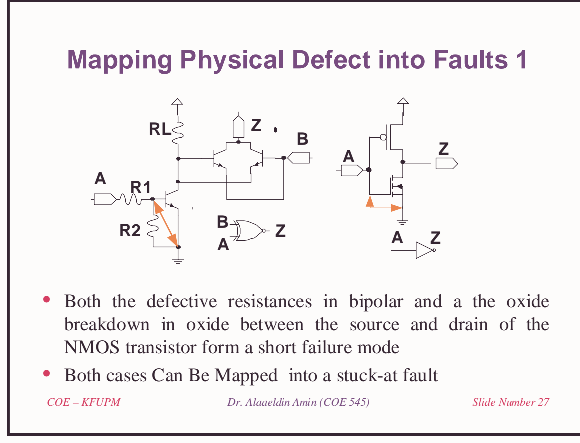
Mapping Physical Defect into Faults 1
RL
Z
B
A
R1
R2
Both the defective resistances in bipolar and a the oxide breakdown in oxide between the source and drain of the NMOS transistor form a short failure mode
Both cases Can Be Mapped into a stuck-at fault
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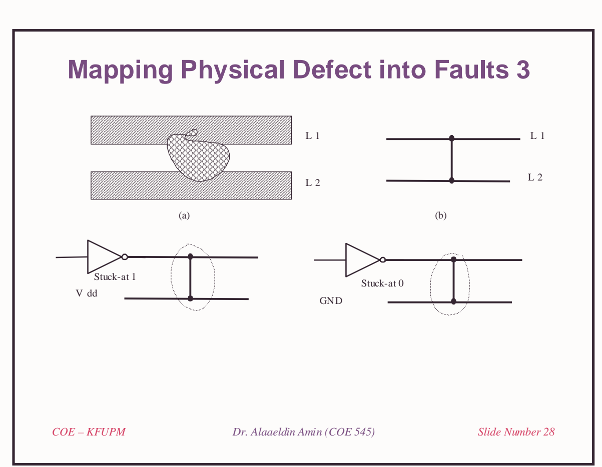
Mapping Physical Defect into Faults 3
L 1
L 2
(a)
(b)
Stuck-at 1
V dd
Stuck-at 0
GND
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Multiple Stuck-at Faults

- A Multiple Stuck-at fault → any set of lines is stuck-at some combination of (0,1) values.

For a Circuit Having L lines, The Number of Possible Faults is

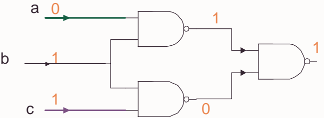
  - 2L Single-Stuck Faults
  - ${}^{L}C_2$ Double-Stuck Faults ≈ $L^2/2$

- In General, the total number of single and multiple stuck-at faults in a circuit with k single fault sites is 3^k-1.
- Statistically, single fault tests cover a very large number of multiple faults.
- With Multiple Faults, a Test for some fault can fail to detect the target fault due to the presence of another→ Masking

Multiple Stuck-at Faults & Fault Masking

Example Fault **C S_@_0** (C/0) is Detectable By TV=011

The Same TV Cannot Detect the Multiple Faults {C/0 , A/1}



Definition: Let Tg be the Set of All TVs that Detect Some Fault *g*. Another Fault *f* is said To *Mask* *g* iff the multiple fault {*f* , *g*} is not detected by any TV in Tg

Bridging Fault Model

- This Model Deals with Shorts Bet 2 Lines
- Behavior of the Shorted Lines is Technology Dependent (Wired-OR && Wired-AND)
- Bridging Faults May Cause an Indeterminate Logic Value at the Faulty Lines (Midway Voltage Level)
- Bridging Faults can cause Feedback Loops Thus Converting a Combinational Circuit into a Sequential One