## Fault Models

- Transistor Stuck ON (S_ON)
  - Transistor Source-to-Drain Shorted independent of the state of the Gate Signal
  - Usually Fault is Considered as a Short Circuit (R=0), but more practically it has a finite resistance R>0
- Transistor Stuck OPEN (S_OP)
  - Transistor Always OFF independent of the state of the Gate Signal → Open Circuit between Source && Drain
  - Usually Considered an ideal Open Circuit (R= ∞), but more paractically it has a finite LARGE resistance R

**Advantages**:

- More Accurate Fault Model Compared to the SSL FM
- Generated TVs, generally Cover Gate-Level SSL Faults

**Disadvantages**:

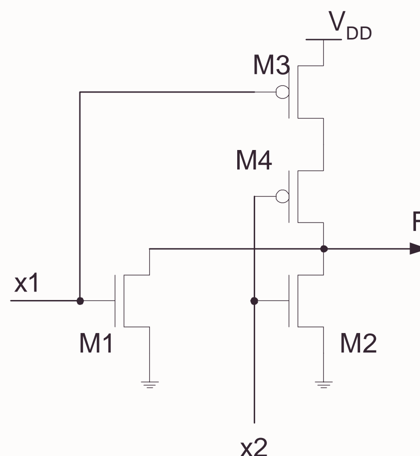
- More Complex Test Generation Algorithms
- SOP Faults Converts the Circuit into a Sequential one



## Stuck-ON (S_ON) Faults

**Example**

- Consider M2 S_ON
- Fault is Provoked (Activated) by Choosing a TV which Should Turn M2 OFF in the FF CUT → x2=0
- Fault is Propagated by Applying x1=0
- IF x1 = 1 Fault Effect is Masked



## Stuck-ON (S_ON) Faults

- Let $R_P$ = ON-Resistance of the PMOS Tr.
- Let $R_N$ = Fault Resistance of the NMOS Tr.
- Faulty O/P Voltage is Given By

$$V_F = \frac{R_n}{R_n + 2R_p} V_{DD}$$

- What is the Fault Effect ?
- How would A & B be Interpreted ? (Logic 0/1)



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## Stuck-ON (S_ON) Faults

- IF Voltage Levels are Used to Test for PO Validity, M2 S_ON Fault May, or May NOT be Detected Depending on the Relative Strength of the PMOS ON-Resistance and the NMOS S_ON Fault Resistance

$$V_F = \frac{1}{1 + 2\,{}^{R_p}\!/_{R_n}} V_{DD}$$



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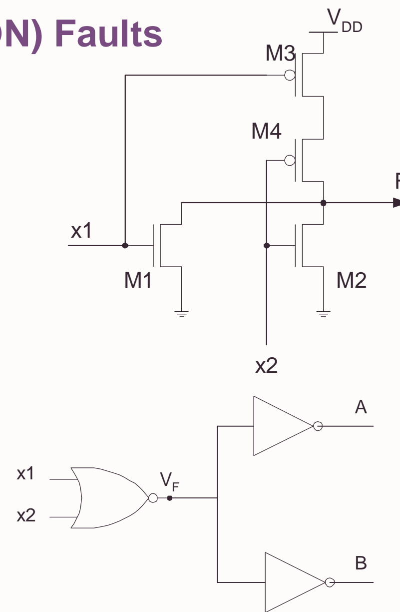
## Stuck-ON (S_ON) Faults

**Conclusion**

- **S_ON Faults May NOT be Detectable if Only the Node Logic Levels are Monitored**

**Solution**

- **Instead of Monitoring Node Voltage Levels, the Static (DC) Current Can Be Monitored → $I_{DDQ}$ Tests**






## $I_{DDQ}$ Tests

- $I_{DDQ}$ = Quiscent (DC/ Steady State /Static) Current Drawn From the $V_{DD}$ Power Supply
- $I_{DDQ}$ = Current Flowing in CMOS CKT when All Nodes are Quiscent (Static)
- $I_{DDQ}$ = 0 (except for leakage) for Fault-Free CMOS Logic
- $I_{DDQ}$ Testing: Refers to Test Techniques which Monitor the Static (DC)Current Drawn by the CUT
- ***Typical Normal $I_{DDQ}$ values ~ Nano Amps***
- ***Abormal $I_{DDQ}$ values ~ Micro Amps***
- $I_{DDQ}$ Tests Can be Either ***External*** or ***Built-In***

# $I_{DDQ}$ Tests

**Advantages**

1. Inexpensive Test Generation
2. Detects a Variety of Fault Types that are not Detectable by Voltage monitoring

**Disadvantages**

1. Longer Application Time / TV
2. Some Faults escape Detection
3. Either Area & Performance Overhead (Built-In $I_{DDQ}$ Test) Or Large Current Resolution (External $I_{DDQ}$ Test)



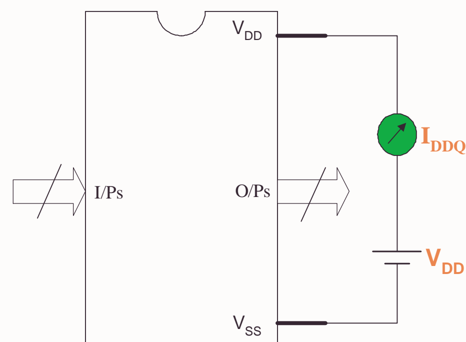
# External $I_{DDQ}$ Tests

**Disadvantages**

- **Large Current Resolution (*Low Sensitivity*)**
- **Slow Testing Speed**

**Advantages**

- **Can be Coupled with Boundary Scan to Test all ICs on a PCB**



# Built-in $I_{DDQ}$ Tests

- **Uses Built-In Current Sensor (BICS) Circuitry**
- **Each Monitored Circuit Module is Augmented with a BICS**

**Advantages**

- **Fine Current Resolution (*High Sensitivity*)**
- **Higher Test Speed**

**Disadvantages**

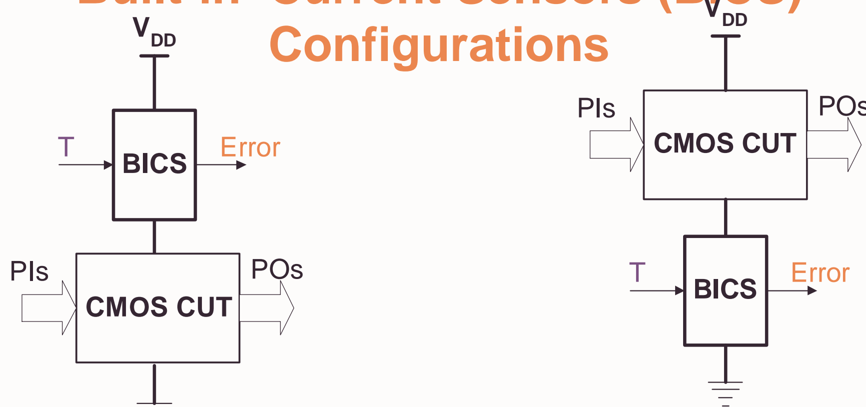
- **Performance & Area Overhead (BICS & test logic)**

**Statistical Data**

- **5000 SRAM Chips were Tested**
  1. **443 Chips Failed Functional Test**
  2. **697 Failed $I_{DDQ}$ Test → Failing Parts Included The above 443 Parts + *254 other Bad Parts that were not caught by the Functional Tests*** *(see "$I_{DDQ}$ Benefits" by Steven D. McEuen in "Bridging Faults and $I_{DDQ}$ Tests" by Y.K. Malaiya, et.al.)*



# Built-in Current Sensors (BICS) Configurations




- T is a Mode Control Signal
  - T=1 → Test Mode
  - T=0 → Normal Operating Mode
- BICS equivalent Resistance Should be Minimized So as not to Severly Degrade CUT Performance

## Faults Detectable by $I_{DDQ}$ Tests

- Stuck-on faults & Bridging
- Break faults
  - Line break
  - Gate break
  - Drain break
  - Source break
- Transistor Stuck-Open faults
- Other faults

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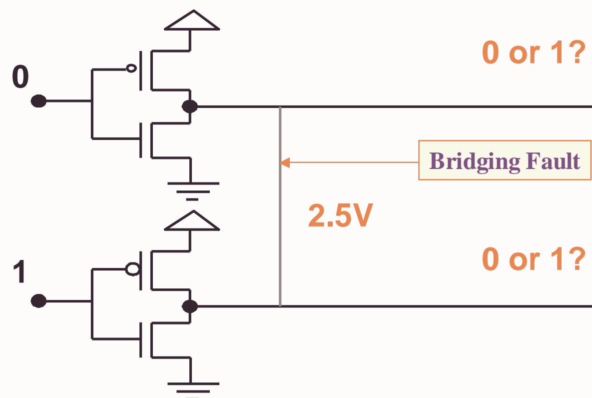
## Bridging Faults




→ Logic monitoring is inadequate !

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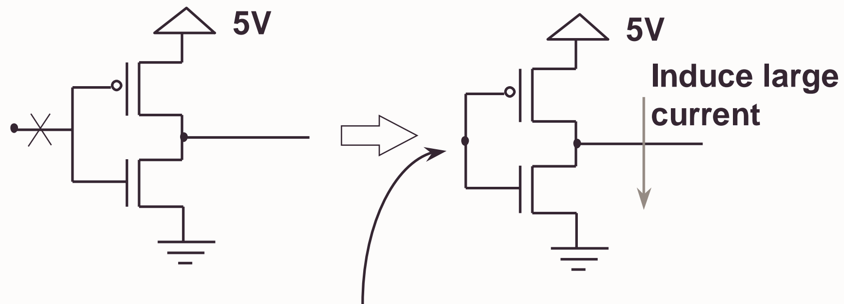
## Line Break Faults




A floating node may drift to 1.5V~3.5V and hence may turn on both PMOS and NMOS transistors

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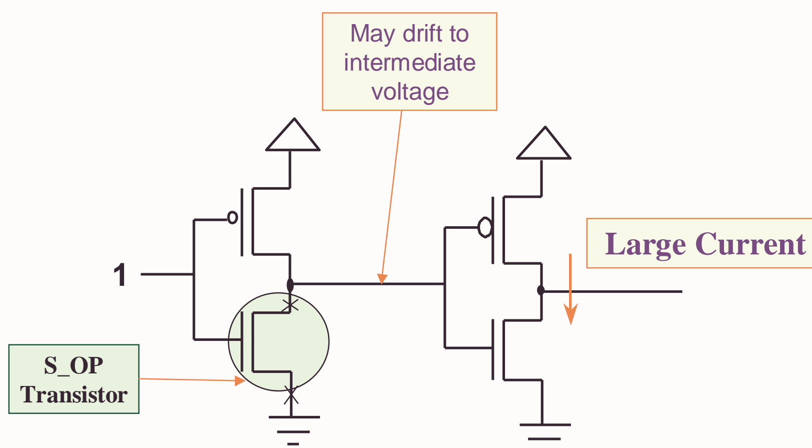
## Source or Drain Break or Transistor Stuck-Open Faults

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## Other Faults That Can Be Detected

- Gate-oxide short (Hawkins ITC85, D&T 86)
- Most stuck-at faults (Fritzmeyer ITC-90)
- Latch-up
- Delay faults
- Any other fault due to extra conductor, missing isolating layer, excess well/substrate leakage, etc.

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## Circuit Constraints

To ensure IDDQ detectability, two conditions must be satisfied:

1. Normal IDDQ must be small
2. Faults must result in large IDDQ (BICS Sensible)

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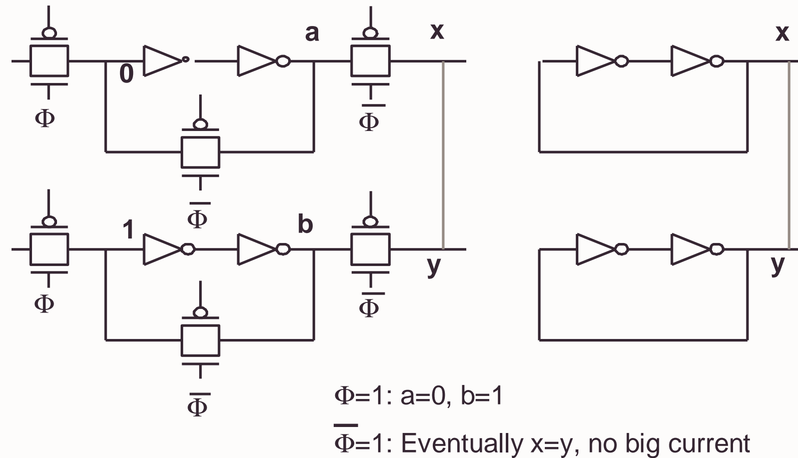
## A BF That Cannot Be Detected By IDDQ



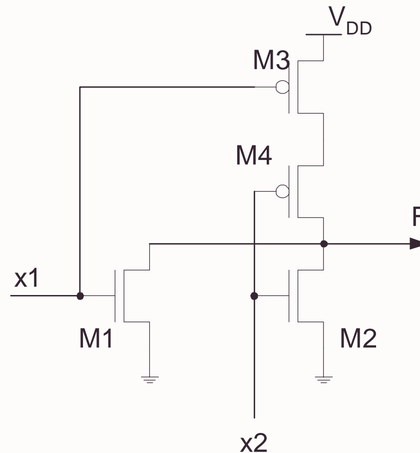

**Problem due to feedback loop**



## Stuck-OPEN (S_OP) Faults

**Consider the Fault M2 S_OP**

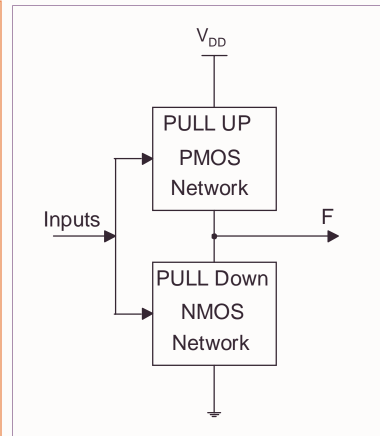
- **For Fault Activation Choose a TV which Turns M2 ON in the FF CUT → x2=1**
- **Fault is Sensitized by x1 = 0**
- **F (*Fault-Free*) = 0**
- **F (*Faulty*) = Hi-Z = F*(t-1)***
- ***F Must Be Initialized to A Value Opposite to the Fault-Free Value***
- ***A Sequence of Two TVs is Needed to Detect S_OP Faults***
  1. ***Initialization TV : x1x2=00***
  2. ***Detection TV : x1x2=01***



## Test Generation for Static CMOS Logic Gate-Level Test Generation (Jain-Agrawal)

- Use Gate Level Model for both Pullup & Pull down Networks
- Use AND, OR & NOT in addition to the "B-Block"
  - Series Connection → AND
  - Parallel Connection → OR
  - I/Ps of PMOS Trs → Complemented Since PMOS is ON iff I/P=0
  - O/P of NMOS Gate NW = S0

  *(Implements the 0's of the Function)*
  - O/P of PMOS Gate NW = S1
  - *(Implements the 1's of the Function)*
  - S0 & S1 are I/Ps of the "B-Block"






## Test Generation for Static CMOS Logic Gate-Level Test Generation (Jain-Agrawal)

| S1 | S0 | O/P of B-Block (Y) |
|---|---|---|
| 0 | 0 | M (*Memory State*) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 (*Contention → PDN assumed Stronger* ) |

- S1 = 1 IFF one or more Paths is enabled in the Pull-Up PMOS NW
- S0 = 1 IFF one or more Paths is enabled in the Pull-Down NMOS NW
- IFF S1S0=11 → *Contention* State, where the O/P depends on the resistance ratio of the pullup to pull down paths.

  → BICS Can Detect Condition
- In Case of Contention, we assumed a stronger Pulldown

## Test Generation for Static CMOS Logic Gate-Level Test Generation (Jain-Agrawal)

- **S_ON, S_OP in CMOS are Translated into SSL Faults in Gate-Level Model**

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## Example

| Tr. Fault | Equiv SSL Fault |
|---|---|
| M1 S_ON (S_OP) | 5/1 (5/0) |
| M2 S_ON (S_OP) | 6/1 (6/0) |
| M3 S_ON (S_OP) | 3/0 (3/1) |
| M4 S_ON (S_OP) | 4/0 (4/1) |
| $x_1$/1 ($x_1$/0) | 1/1 (1/0) |
| $x_2$/1 ($x_2$/0) | 2/1 (2/0) |
| *F*/1 (*F*/0) | 9/1 (9/0) |

**Since only SSL Faults need be Considered → D-Alg, PODEM, FAN may be Used to Derive Tests for these Faults**

**Need The Singular Covers & Propagation D-Cubes of the B-Block**

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