DIGITAL SYSTEM TESTING
COE -545

Lecture - 01

INTRODUCTION

- An Electronic System/Hardware Product (IC, PCB, full System) goes Through Several Stages
- Errors May be Introduced at any Stage
  - System Specification (Human Error) → All fabricated parts will function according to the Erroneous Specs!!!
  - System Design: Designers Error → All parts will exhibit the error
  - Fabrication/Processing (Operator errors, Equipment Problems, Defective Material, etc.)
  - Assembly, Packaging, Integration → Wire Bonding Cracks in Silicon, Bad Die Attach, Shorts, etc.
- Tests/Verification Must be Conducted at all Stages to Ensure an Error-Free Product

Verification vs. Testing

Definitions

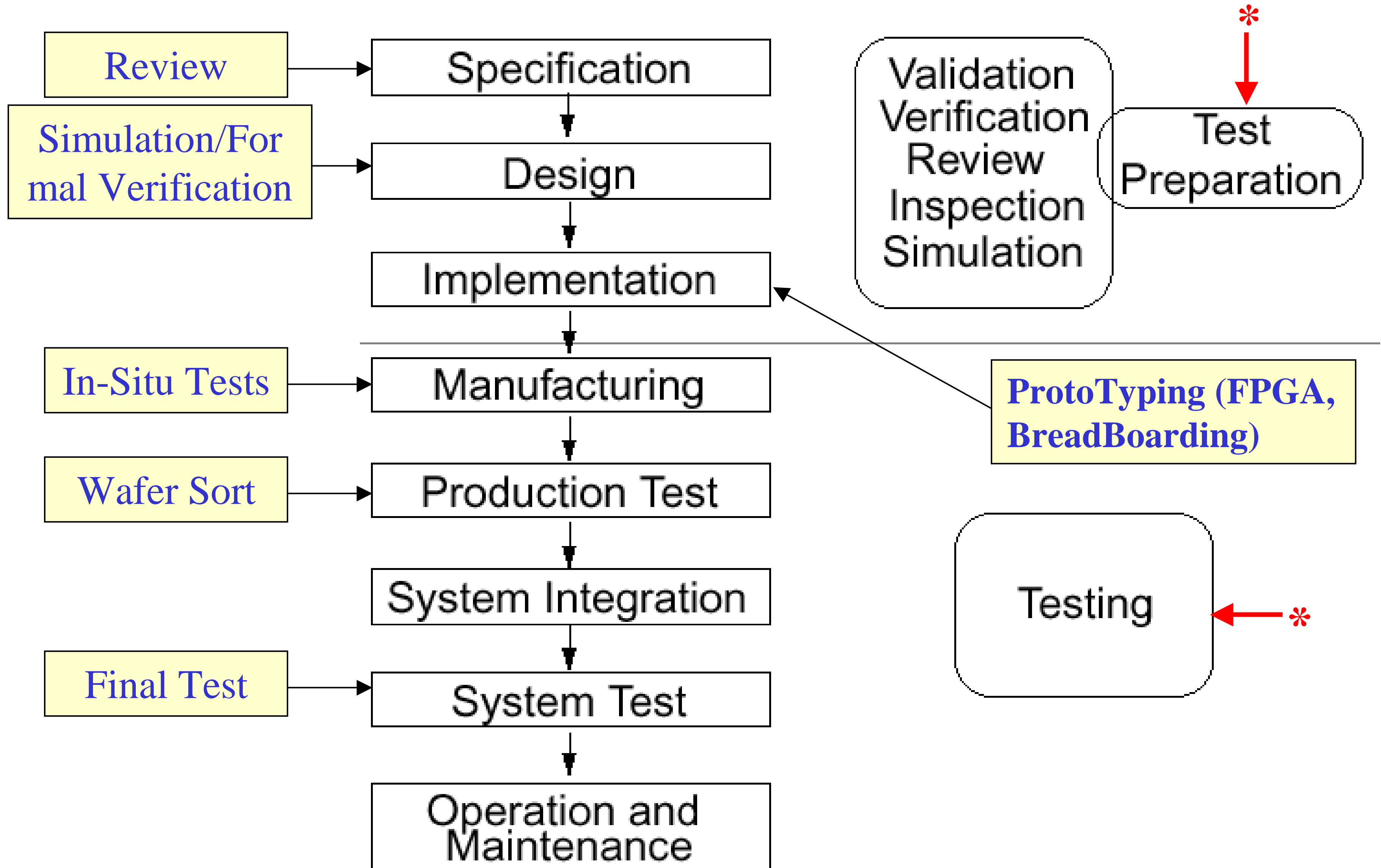
- Design synthesis: Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- Verification: Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- Test: A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

Verification v/s Testing

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

- Verifies correctness of manufactured hardware.
- Two-part process:
  - 1. Test generation: software process executed once during design
  - 2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of product devices.

Hardware Life Cycle



Which Type of Test Are We Interested in This Course ?

- Post Fabrication Tests:
  - Production Test (e.g. Wafer Sort)
  - Final Test (After Integration, Assembly, Packaging) where Faults can be introduced in the final phase, e.g. Silicon Cracks due to wire bonding, Bad Die Attach, Shorts, etc.
- Are we Interested in all Types of these Tests?
  - Nooooooooo
- What Are the Types of Tests Conducted as Final Test?

Types of Tests

1. DC/Parametric Tests: *measures DC Parameters, e.g.* V_{IL} , V_{IH} , V_{OL} , V_{OH} , I_{OL}, I_{OH} , I_{IL}, I_{IH}, *Threshold Voltages, Current Gains, etc.* → *Noooooooooo*
2. AC (Time-Related) Tests: *Speed, Setup/Hold Times,etc.* → *Noooooooooo*
3. Functional Tests: *Validates, in a Cost-Effective Way, If a Given CKT Performs its intended Function* → *Yes … Yes …*
   - *Test Stimuli Are Applied at a Relaxed Frequency (Much Slower Than Normal Speed) To Avoid AC Speed Sensitivities.*

Test Economics

Cost of an Electronic System (*IC, PCB, System*)

1. **Non-Recurring Expenses** (***NRE***) Or **Fixed Cost** → One Time Cost Shared By Whole Production Volume

   - Initial Development Cost:
     - Design
     - Design Verification
     - Prototyping and Debugging

- This Cost Component is Volume independent.

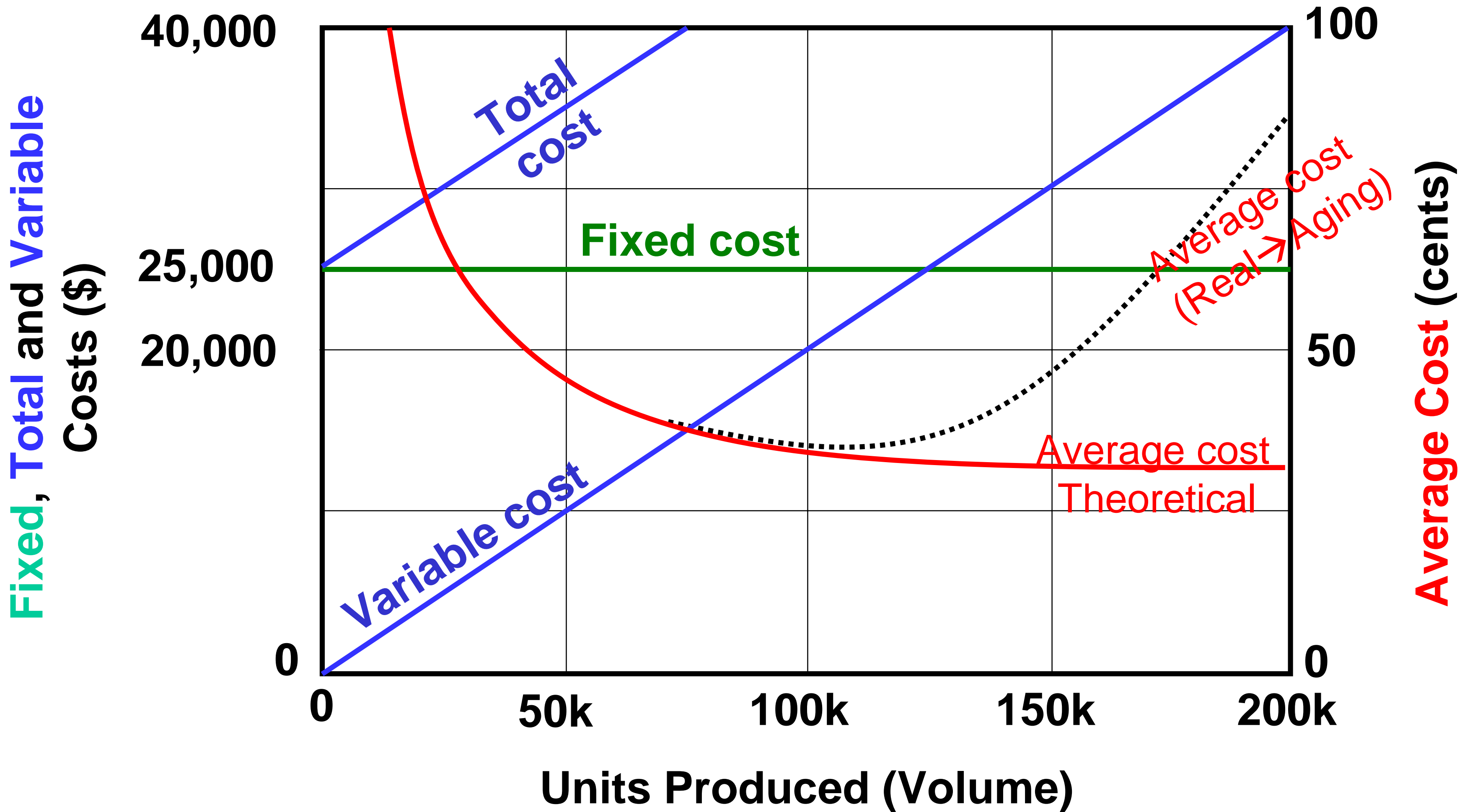
Test Economics

Cost of Electronic System (IC, PCB, System)

2. **Recurring Expenses** → Money Paid Every Time the System Is Fabricated
   - Fabrication Cost
   - Assembly/Packaging Cost
   - Testing Cost
     - Production Test (e.g. Wafer Sort) → Loose Test To Identify Functional Parts
     - Final Test (After Assembly & Before Shipping to Customers) → More Thorough and Costly Test with Full Characterization (Binning?)

- This Cost Component is Volume Dependent
- Higher volumes Result in Higher Recurring Cost

Cost Analysis Graph



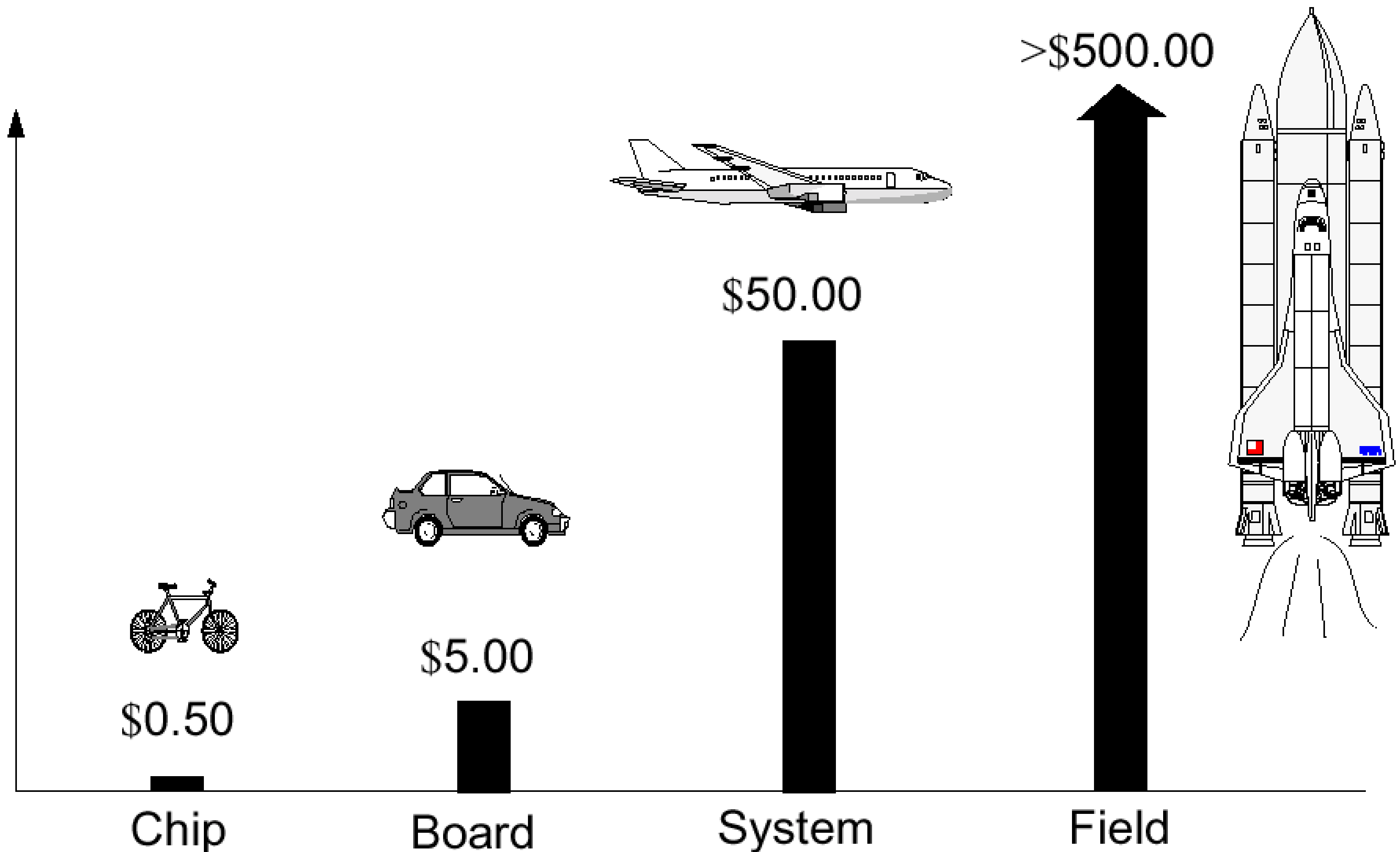
Testing Cost

- Cost Increases Dramatically as Faulty Components Pass w/out Detection to Higher Level of Integration

Rule of 10

- ***It costs 10 times more to test a device as we move to higher level in the product manufacturing process***
  - 1$ To Fix an IC (Throw it out)
  - 10$ To Find and Replace a Defective IC on a PCB
  - 100$ To find a bad PC board in a system
  - 1000$ to find bad component in a fielded System

Cost of Finding Defects (“Rule of Tens”)



Diagnosis vs. Detection

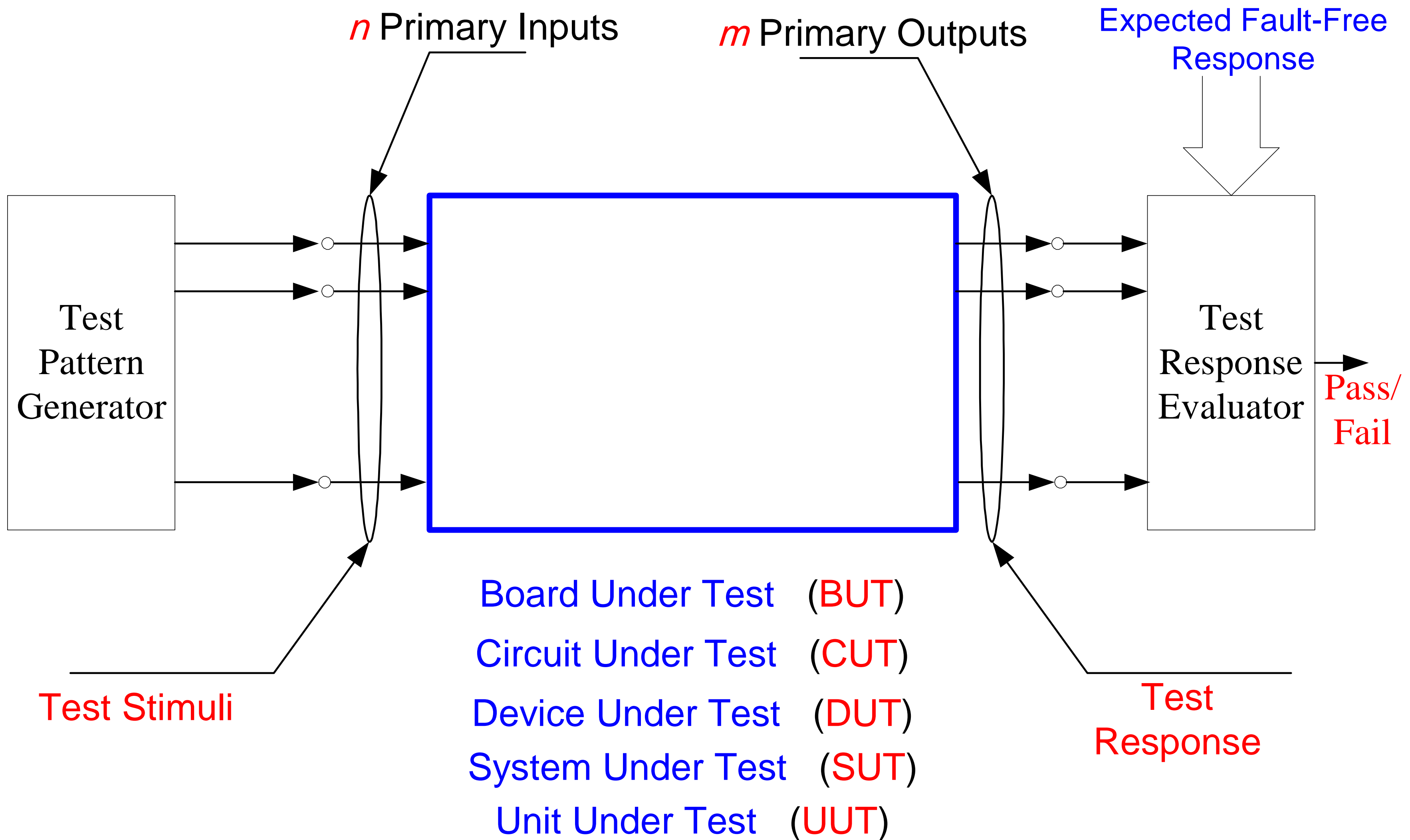
Test Objectives

- PCB's and Systems → Reclaim (*Repair*) Defective Parts → Fault Location (*Diagnosis*) is Required
- IC's → Defective Chips Cannot be Reclaimed (*Repaired*) → Discard
- Fault Location (*Diagnosis*) is *NOT* Required for IC's → Only Fault *Detection* is Needed.
- The More Thorough a Test is, The More Expensive it will Be.

Role of Testing

- Detection: Determination whether or not the *device under test* (DUT) has some fault.
- Diagnosis: Identification of a specific fault in a faulty product.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- Failure mode analysis (FMA): Determination of manufacturing process errors that may have caused defects to be introduced in the Products.

Test Arrangement



Terminology

- Primary Inputs (PIs): Inputs That Can Be Externally Driven/Controlled
- Primary Outputs (POs): Outputs That Can Be Externally Monitored/Observed
- Test Vector/Pattern (TV): The Set of Stimuli Applied to the PIs and Their Expected Fault-Free POs Response.
- Test Sequence: A Sequence of TVs

Automatic Test Equipment (ATE)

- Is a Sophisticated Equipment Designed to Test Complex Electronic System
- It Usually Incorporates
  - Programmable Test Pattern Generator
  - Programmable Test Response Evaluator
  - Memory to Hold Expected Fault-Free Response
- Can Perform Parametric (DC) as well as AC (Timing) and Characterization Tests

ADVANTEST Model T6682 ATE

T6682 ATE Specifications

- **Uses 0.35 μm VLSI chips in implementation**
- **1024 pin channels**
- **Speed: 250, 500, or 1000 MHz**
- **Timing accuracy: +/- 200 ps**
- **Drive voltage: -2.5 to 6 V**
- **Clock/strobe accuracy: +/- 870 ps**
- **Clock settling resolution: 31.25 ps**
- ***Pattern multiplexing*: write 2 patterns in one ATE cycle**
- ***Pin multiplexing*: use 2 pins to control 1 DUT pin**

LTX FUSION HF ATE

Specification

- **Intended for SOC test – digital, analog, and memory test – supports scan-based test**
- **Modular – can be upgraded with additional instruments as test requirements change**
- **enVision Operating System**
- **1 or 2 test heads per tester, maximum of 1024 digital pins, 1 GHz maximum test rate**
- **Maximum 64 Mvectors memory storage**
- **Analog instruments: DSP-based synthesizers, digitizers, time measurement, power test, *Radio Frequency* (RF) source and measurement capability (4.3 GHz)**

Test Application

- **External** (*Off-chip*) **Vs Built-In** (*on-chip*) **Testing**
- **External (Off chip)Testing**:
  - Requires *Expensive* **ATE** that is independent of the **DUT**
  - **TVs** Applied Externally & Evaluated Externally by **ATE**

- **Built-In (On chip)Testing** :
  - Test Pattern Generator Circuitry is built into the **DUT** itself
  - If Response Evaluator is built into the **DUT** → Self-Testing/Self-Checking
  - Inexpensive
  - Performance & Area overhead
  - At-System Speed Testing

Test Application

Expensive Tester

High Bandwidth

Source/
sink

Logic

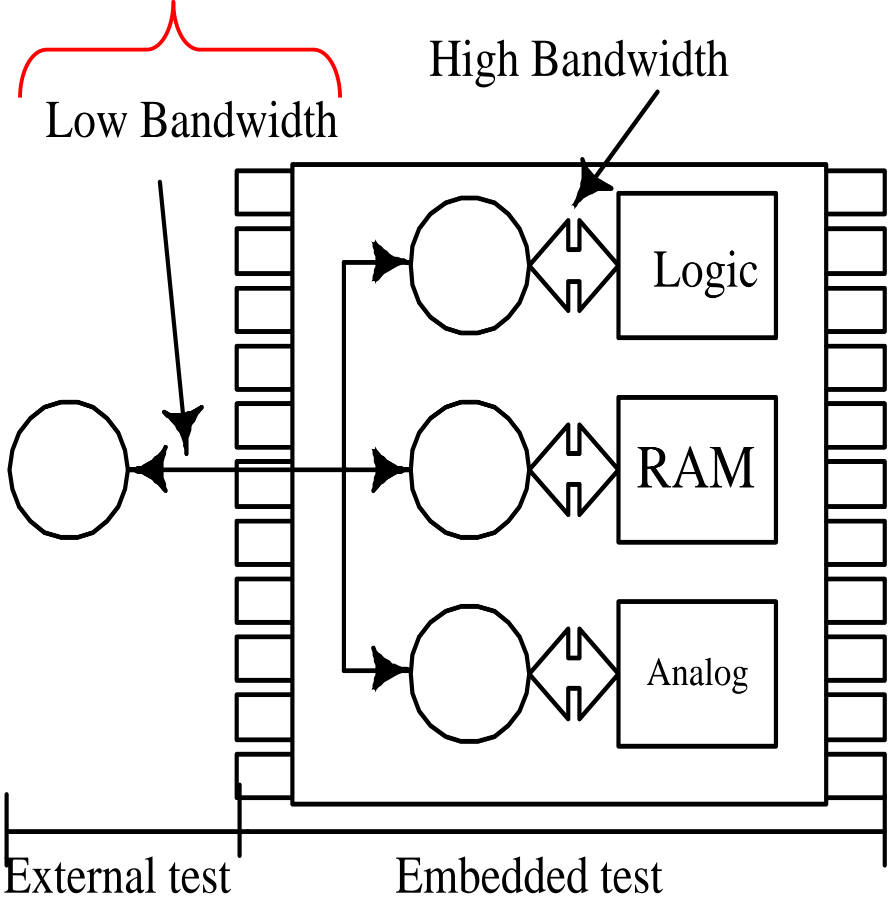
RAM

Analog

External test

Embedded test

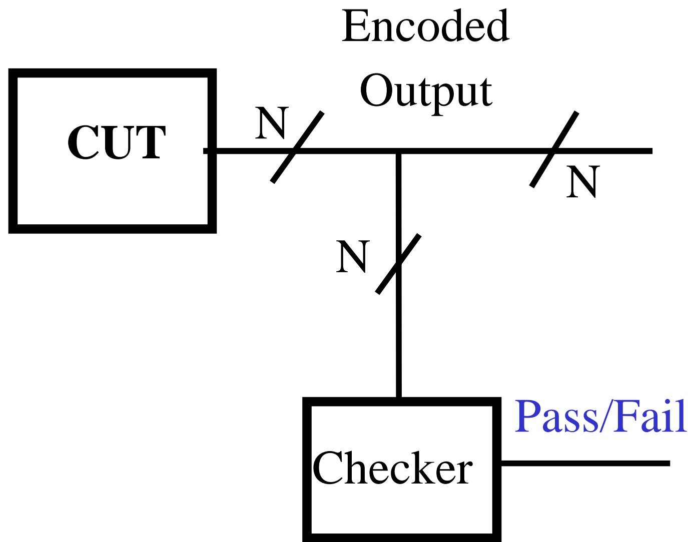
Inexpensive Tester



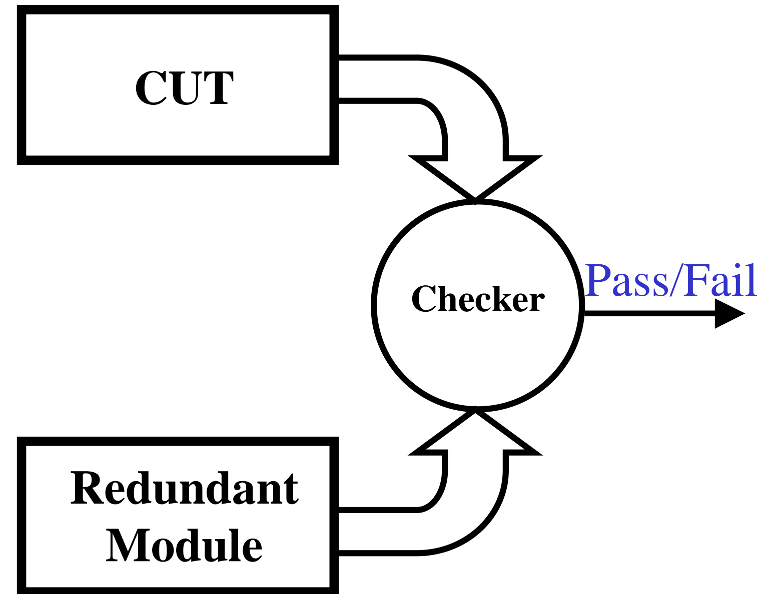
Test Application Mode

- **On-Line** (IMPLICIT) **Vs Off-Line** (EXPLICIT) **Testing**
- **On-Line** (IMPLICIT) **Testing**:
  - Testing conducted during Normal System Operation
  - No TVs Applied during Normal System Operation
  - Monitoring Certain System Properties which should remain Invariant through Fault-Free Operation
    - Only One Decoder Output Is Selected at any Time
    - Only Legal Op-Codes Are Allowed
  - Such Properties Not Easily-Defined
  - Reliable Design Techniques are Usually Employed (e.g. Adding Redundancy)
    - Information Redundancy: Use of Parity Bits And/Or Error detecting&Correcting Codes
    - Modular (Hardware) Redundancy: Replicating Certain Modules and Check for Identical Outputs.

On-Line Testing



On-Line Testing
with Information
Redundancy



On-Line Testing
with Hardware
Redundancy

Test Application Mode

- **OFF-Line** (EXPLICIT) **Testing** :
  - If System is Designed for Testability, the System has 2 Modes:
    - Normal Mode : Normal System Operation
    - Test Mode : Predetermined Set of TVs are Applied
  - Both Modes are Mutually Exclusive → Cannot be Run Concurrently