Bridging faults and I_{ddq} testing

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Outline:

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- What is I_{ddq} testing?
- Why I_{ddq} testing?
- Example
- Results
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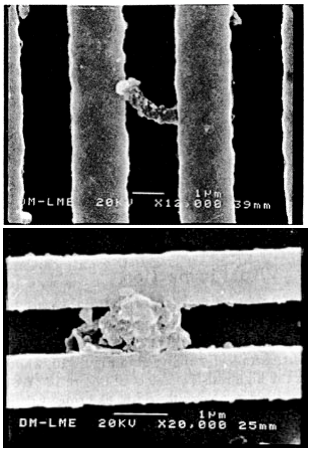
Bridging faults

- Definition: A bridging fault occurs when two leads in a logic network are connected accidentally
- Most common defect in Integrated Circuits (up to 30%)



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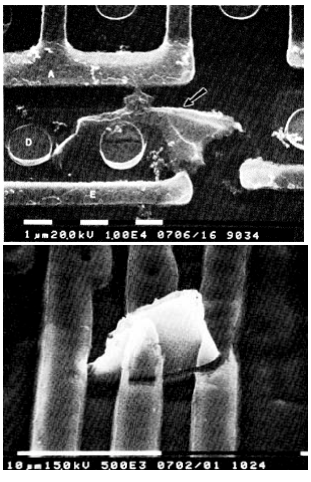
Bridging faults (cont.)

- Can be divided into three classes
  - Bridging within a logic element
  - Bridging between logical nodes without feedback
  - Bridging between logical nodes with feedback



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What is I_{ddq} testing?

- The test of quiescent supply current (I_{ddq})
- Faults and defects will result in elevated I_{ddq} current
- Built-in current sensor can be used

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Why I_{ddq} testing?

- Stuck-at fault model has problems in representing CMOS failure modes (bridging faults, stuck-on faults, etc..)
- In the case of bridging faults, one logic value does not always dominate the other, therefore, cannot be tested by logic testing (depends on bridging resistance)

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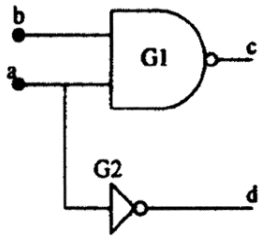
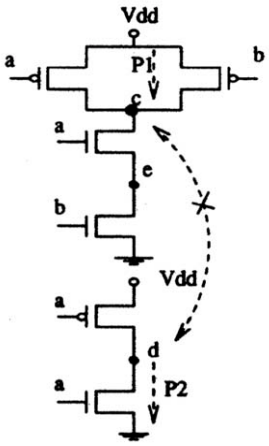
I_{ddq} tests for bridging faults

- An example
  a=1, b=0 a=0, b=0





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I_{ddq} tests for bridging faults (cont.)

- General rule for identifying I_{ddq} tests for a bridging fault between nodes x and y:
  - *An input vector T is an I_{ddq} test for (x,y) if and only if T(x) not equal to T(y)*

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Results - Comparison between Stuck-fault testing and I_{ddq} testing

- International Symposium on Circuits and Systems (ISCAS) benchmarks

Name	# Trans-istors	# nodes	# inputs	# outputs	# gates	# gate types
C17	26	21	5	2	6	1
C432	728	421	36	7	174	12
C499	1396	822	41	32	180	7
C880	1164	657	60	26	304	12
C1355	1768	949	41	32	577	10
C1908	2058	1132	33	25	332	13

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•Results (cont.)

Name	Patterns	Faults	Missed	% Detected
C17	6	74	1	98.7%
C432	53	3968	174	95.6%
C499	58	7806	362	95.4%
C880	67	7909	99	98.8%
C1355	87	12103	62	99.5%
C1908	108	14023	338	97.6%

Stuck fault patterns

Name	Patterns	Faults	Missed	Coverage
C17	5	74	0	100.00%
C432	40	3968	56	98.59%
C499	99	7806	1	99.99%
C880	27	7909	2	99.97%

Current sensing

- Current test detects a higher percentage of bridging faults than stuck fault testing

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Results (cont.)

- Detecting faults using current sensing is easier than in stuck fault testing
  - Inputs need not be propagated to outputs
  - Transistor sizing is not a factor in current testing

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Disadvantages

- Slow, because have to wait for circuit to be stable to measure current
- Overhead in chip area for current monitor circuit
- Different leakage current limit for different circuits

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Conclusion

- Very effective technique, more accurate model
- Provide higher fault coverage than logic testing

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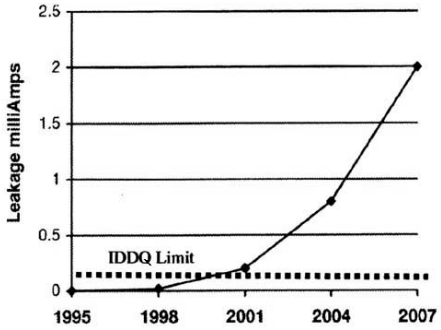
Future work

Limitation of I_{ddq} testing

- As technology shrinks, leakage current increase
- Classical I_{ddq} testing will fail below 0.18 micron ?
- Delta-I_{ddq}, I_{ddt}, current signatures, power consumption analysis?



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