# Testing the Interconnect of Xilinx 4000 Series FPGAs

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• March 18, 2000

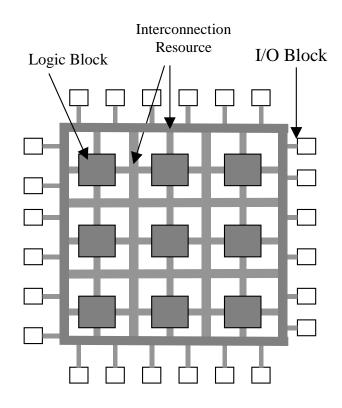
## Outline

- Problem Statement
- Previous Work
- Features of BIST for FPGAs
- Proposed Test Strategies
- Conclusion
- Future Work

## Problem Statement

- Limitations of Read-back Check Features
- Limitations of JTAG port for FPGAs
  - Speed
  - Do not support INTEST mode
- In-system test solutions
  - Independent of intended system functions
  - Minimal number of test configurations

# FPGA Architecture

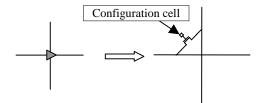


## Programmable Interconnect Resources

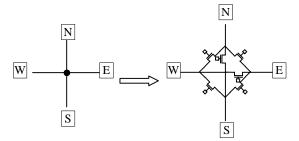
- Programmable switches
- Routing resources
  - Global routing resources
  - Local routing resources
- Buffers and pull-up transistors

# Programmable Switches

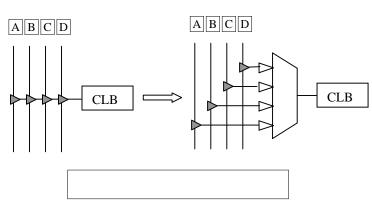
• Basic programmable switch



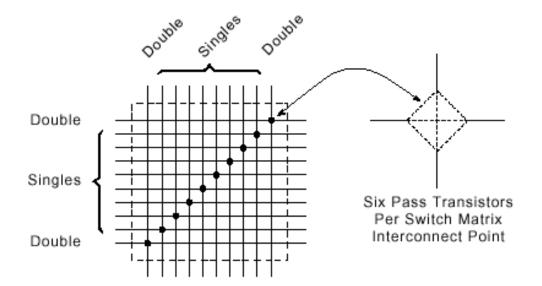
Cross-point PS



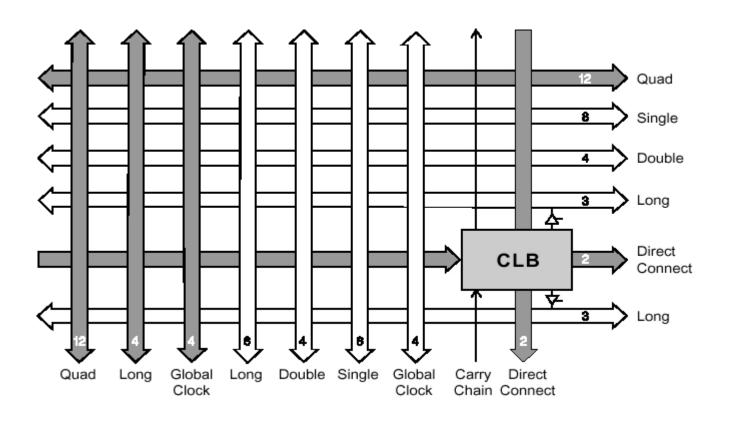
• Multiplexer PS



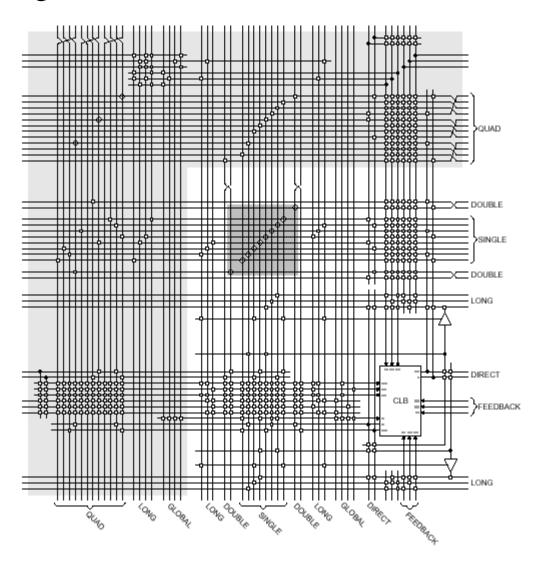
# Programmable Switch Matrices



## High Level Routing Diagram



#### Detail of Programmable Interconnect associated with a CLB



#### Previous Work

- Mainly for device testing
  - Full access of I/O pins
  - Externally applied test patterns
- Taking advantage of homogeneous array structure
- Make use of the reprogrammability
- Only one BIST solution
- All for university research
  - Just test simple operation mode
  - Do not test dedicated features

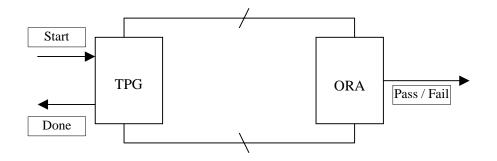
## **BIST** Procedure

- Reconfigure the FPGA to create TPGs, WUTs and ORAs.
  - WUTs are tested concurrently as many as possible within the limitation of the routing and logic resources of the FPGA
- Initiate the test.
- Generate test patterns
  - Exhaustive/Pseudo-exhaustive test patterns because the number of s WUTs is relatively small.
- Analyze the response
- Read the test result.

### Features of BIST for FPGAs

- Two types of inputs
  - $-\mathbf{C}^{\text{MTP}} = \mathbf{C}^{\text{TS}} \times \mathbf{C}^{\text{TC}}$ 
    - Every component must be used(tested) at least once
    - test patterns must cover all the faults in the fault model
- Zero Overhead
- Test in Parallel
- Exhaustive/Pseudo-exhaustive test patterns
- Focus on minimum number of test configurations
- Often use Comparison-based Approach

## Comparison-Based BIST Strategy



- Idea:
  - ORA compares the patterns propagating on the two WUTs which should be identical if their propagation is not affected by faults
- Advantages / Disadvantages of Comparison-based approach
  - Advantages
    - No alias
    - high fault coverage
  - Disadvantage
    - not so strong multiple-fault detectability

## Our Porposed Approaches

- Achieve strong multi-fault detectability
- Explore dedicated features of FPGAs
  - Wide MUX, wired-AND busses
  - Wide edge decoder
- Employ novel techniques
  - error-detecting code
  - MUX structure
- Three-step approach
  - Test global routing resources with minimum configurations
  - Test local routing resources with minimum configurations
  - Merge the testing of global and local routing resources under minimum configurations

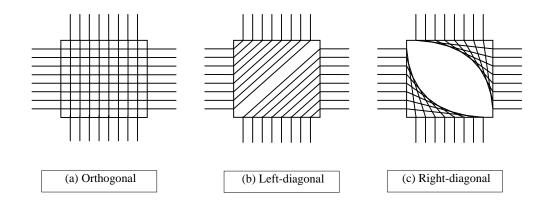
## Fault Models

- multiple segment stuck-at 0/1 faults;
- multiple segment stuck-open faults;
- multiple bridge faults;
- multiple switch stuck on/off faults;
- the combinations of the above faults.

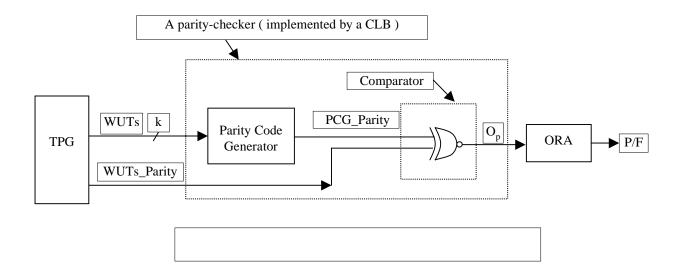
## Test Global Routing Resources

#### • Idea:

 Connect wiring segments using programmable switches to form busses, then application bus testing techniques (need some modification)



# Parity Checking Circuitry



## Analysis of Multi-fault Detectability

- Parity-checking approach vs Comparison-based approach
- A more powerful approach: MUX architecture.

#### Conclusion

• Under the proposed approach, it requires a minimum of six test configurations to test the global routing resources of Xilinx 4000E/X FPGAs. The proposed approach provides superior multiple fault coverage compared with comparison based approach.

#### Future Work

• Development of testing strategies for local and I/O routing routing resources and unifying these test strategies.