COE 405, Term 041

COE 561 Digital System Design and Synthesis

HW# 5

Due date: Sunday, Dec. 26

Q.1. Consider the binding of a network implementing the conjunction of 10 variables. Assume that the available cells are only two-input AND gates with cost 2, three-input AND gates with cost 3 and four-input AND gates with cost 4.

(i) Find an optimum cover of the tree decomposition of the network given below using 2-input AND gates as base functions:

$k = a\ b;$	$l = i\ j;$	$m = k\ c;$	$n = d\ e$
$o = f\ g;$	$p = h\ l;$	$q = m\ n;$	$r = o\ p$
s = q r			

(ii) Is this the best implementation of the given network with the available cells? Is there decomposition into the same base function leading to a lower cost solution?

(iii) Show all the partitions trees for the 4-input AND gate cell that need to be stored in the library assuming the use of 2-input AND gates as base functions.

(iv) Show all the ROBDDs for the 4-input AND gate cell that need to be stored in the library for Boolean matching.

Q.2. Consider a library containing the following cells:

Cell	Area Cost
INV	2
NAND2	3.5
NOR2	3
AOI21	4
AOI22	5
OAI21	4
OAI22	5

Assume that we have the following network:

[1] = a' b';	*[2] = d e;*	*[3] = h + i;*	*[4] = k + l;*
[5] = [4] + j';	*[6] = [1] c;*	*[7] = [2] + [3]';*	*[8] = [5] m;*
[9] = [3] + g;	*[10] = [8] + n';*	*X = [6] [7];*	*Y = [9] f';*
Z = [3] [10]			

(i) Show the pattern trees of the library cells using NAND2 and INV as base functions.

(ii) Decompose the given network using the base cells NAND2 and INV.

(iii) Partition the decomposed network into subject graphs.

(iv) Find a minimal cover (in terms of area) based on the given library for each subject graph using dynamic programming approach.

(v) One way to improve mapping is to insert pairs of inverters at each line in the subject graph and then find an optimal mapping of the subject graph. Any mapped pair of inverters can then be eliminated. Using this technique is it possible to obtain a better mapping of the given network.

(vi) Using the given library, use the sis command ***read_libray*** to read the library. Then, map the network to the library using the sis command ***map –s –m 0***. Compare your solution to the solutions obtained in (iv) & (v). You can save the mapped circuit using the sis command ***write_blif –n***.

NOTE: Do not simplify the given network and map it as given. Its only purpose is to illustrate the various issues associated with cell-library binding.