Curriculum Vitae

Aiman H. El-Maleh

Personal Details

Current address:	Department of Computer Engineering King Fahd University of Petroleum & Minerals P.O. Box 1063, Dhahran 31261, Saudi Arabia
WWW:	http://faculty.kfupm.edu.sa/COE/aimane
E-mail:	aimane@kfupm.edu.sa
Phone:	+966 (3) 860-2811
Fax:	+966 (3) 860-3059
Office:	Building 22, Room 405-7

Education

McGill University, Canada	PhD Degree (Dean's honor list), 1995 Thesis title: "Testability Preservation of Combinational and Sequential Logic Synthesis Transformations."
University of Victoria, Canada	M.A.Sc., Electrical Engineering, 1991 Thesis title: "Image Compression using One-Dimensional Vector Quantization."
KFUPM, Saudi Arabia	B.Sc., (First Hon.), Computer Engineering, 1989

Scholarships and Awards

Distinguished Advising Award	College of Computer Sciences & Engineering, KFUPM, 2017/2018.
Excellence in Research Award	KFUPM, 2015/2016
Distinguished Advising Award	College of Computer Sciences & Engineering, KFUPM, 2013/2014.
Distinguished Teaching Award	College of Computer Sciences & Engineering, KFUPM, 2011/2012.
Excellence in Research Award	KFUPM, 2010/2011.
First Instructional Technology Award	KFUPM, 2009/2010.
Distinguished Teaching & Advising Award	College of Computer Sciences & Engineering, KFUPM, 2006/2007.
Distinguished Teaching & Advising Award	College of Computer Sciences & Engineering, KFUPM, 2001/2002.
DATE Best Paper Award	Winner of the best paper award for the most outstanding contribution in the field of Test at the Design Automation and Test in Europe (DATE)

	Conference, 1995.
Max Binz Fellowship	McGill University, 1993-94
FCAR Scholarship	McGill University, 1993-94
NSERC Scholarship	McGill University, 1991-93
University of Victoria Fellowship	University of Victoria, 1990-91
University of Victoria Best TA Award	University of Victoria, 1990

Employment Summary

Professor: June 2017 to present, King Fahd University of Petroleum and Minerals.

Associate Professor: Jan. 2009 to May 2017, King Fahd University of Petroleum and Minerals.

Assistant Professor: 08/98 to 12/2008, King Fahd University of Petroleum and Minerals
Taught the following courses: Fundamentals of Computer Engineering (COE 200 & COE 202), Computer Organization and Assembly Programming (COE 205), Computer Architecture (COE 308), Data and Computer Communications (COE 342), VLSI System Design (COE 360), Design and Modeling of Digital Systems (COE 405), Digital System Testing (COE 464 & COE 545), Synthesis of Digital Systems (COE 561), Seminar (COE 390) and COE Cooperative work (COE 351).

Member of Scientific Staff: 05/95 to 08/98, Mentor Graphics Corporation, Wilsonville
Involved in developing advanced Built-In Self Test techniques for ASICs with embedded cores and high performance data path architectures, with feasibility study on the Intel P6 microprocessor. Furthermore, involved on research and development of partial scan selection algorithms for one-million plus gates designs. In addition, developed a fast sequential learning technique for sequential circuits and demonstrated its applicability in improving the performance of sequential ATPG.

Publications

Journals

1) Ghashmi H. Bin Talib, Aiman H. El-Maleh, and Sadiq M. Sait, “Design of Fault Tolerant Adders: A Review,” The Arabian Journal for Science and Engineering, 2018. [IF=1.092, Q3]
2) Ahmad T. Sheikh, Aiman H. El-Maleh, "Double Modular Redundancy (DMR) Based Fault Tolerance Technique for Combinational Circuits," Journal of Circuits, Systems, and Computers, Volume No.27, Issue No. 6, 2018. [IF=0.595, Q4]
3) Aiman H. El-Maleh, "A Finite State Machine Based Fault Tolerance Technique with Enhanced Area and Power of Synthesized Sequential Circuits," IET Computers & Digital Techniques, Volume 11, Issue 4, July 2017, pp. 159 – 164. [IF=0.639, Q4]
4) Ahmad T. Sheikh, Aiman H. El-Maleh, "An Integrated Fault Tolerance Technique for Combinational Circuits Based on Implications and Transistor Sizing," Integration, the VLSI Journal, Volume 58, June 2017, pp. 35–46. [IF=0.904, Q4]
5) Aiman H. El-Maleh, "A Probabilistic Pairwise Swap Search State Assignment Algorithm for Sequential Circuit Optimization," Integration, the VLSI Journal, Volume 56, Jan. 2017, pp. 32–43. [IF=0.904, Q4]
6) Ahmad T. Sheikh, Aiman H. El-Maleh, Muhammad E.S. Elrabaa, and Sadiq M. Sait, "A Fault Tolerance Technique for Combinational Circuits Based on Selective-Transistor Redundancy," IEEE Transactions on VLSI, Vol. 25, Iss. 1, Jan. 2017, pp. 224-237. [IF=1.744, Q2]
7) Muhammad E. S. Elrabaa, Amran Al-Aghbari, Mohammad Al-Asli, Aiman El-Maleh, Abdelhafid Bouhraoua, Mohammad Alshayeb, "A low-cost Platform for the Prototyping and

Characterization of Digital Circuit IPs," Integration, the VLSI Journal, Volume 54, June 2016, Pages 1–9. [IF=0.904, Q4]

8) Aiman H. El-Maleh, "Majority-Based Evolution State Assignment Algorithm for Area and Power Optimization of Sequential Circuits," IET Computers & Digital Techniques, Vol. 10, Iss. 1, pp. 30–36, 2016. [IF=0.639, Q4]
9) Sadiq M. Sait, Abubakar Bala, Aiman H. El-Maleh, "Cuckoo Search Based Resource Optimization of Datacenters," Applied Intelligence, April 2016, Volume 44, Issue 3, pp 489-506. [IF=1.983, Q2]
10) Aiman H. El-Maleh and Khaled A.K. Daud, "Simulation-Based Method for Synthesizing Soft Error Tolerant Combinational Circuits," IEEE Transactions on Reliability, Volume 64, Issue 3, Sep. 2015, Pages 935 - 948. [IF=2.729, Q1]
11) Aiman H. El-Maleh, Sadiq M. Sait, Abubakar Bala, "State Assignment for Area Minimization of Sequential Circuits Based on Cuckoo Search Optimization," Computers & Electrical Engineering, Volume 44, May 2015, Pages 13–23. [IF=1.747, Q2]
12) Mohammad Alshayeb, Muhammad E. S. Elrabaa, Ayman Hroub, Amran Al-Aghbari, Aiman H. El-Maleh and Abdelhafid Bouhraoua, "Towards a Test Definition Language for Integrated Circuits," Journal of Circuits, Systems, and Computers, Volume No.24, Issue No. 3, 2015. [IF=0.595, Q4]
13) Aiman H. El-Maleh, Ayed S. Al-Qahtani, "A Finite State Machine Based Fault Tolerance Technique for Sequential Circuits," Microelectronics Reliability, Volume 54, Issue 3, March 2014, Pages 491-662. [IF=1.236, Q3]
14) Aiman H. El-Maleh, Feras Chikh Oughali, "A Generalized Modular Redundancy Scheme for Enhancing Fault Tolerance of Combinational Circuits," Microelectronics Reliability, Volume 54, Issue 1, January 2014, Pages 316–326. [[IF=1.236, Q3]
15) Aiman H. El-Maleh, Ahmad T. Sheikh and Sadiq M. Sait, "Binary Particle Swarm Optimization (BPSO) Based State Assignment for Area Minimization of Sequential Circuits," Applied Soft Computing, Volume 13, Issue 12, December 2013, Pages 4832–4840. [IF=3.907, Q1]
16) Sadiq M. Sait, Ahmad T. Sheikh, Aiman H. El-Maleh, "Cell Assignment in Hybrid CMOS/Nanodevices Architecture Using a PSO/SA Hybrid Algorithm," Journal of Applied Research and Technology, Vol. 11, October 2013, pp. 653-664. [IF=0.447, Q4]
17) Aiman H. El-Maleh, Mohamed Adnan Landolsi and Esa A. AlGhoneim, "Window-Constrained Interconnect-Efficient Progressive Edge Growth LDPC Codes," International Journal of Electronics and Communications, Volume 67, Issue 7, July 2013, Pages 588–594. [IF=2.115, Q2]
18) Wenfa Zhan and Aiman H. El-Maleh, " A New Scheme of Test Vector Compression Based on Equal-Run-Length Coding (ERLC)," Integration, the VLSI Journal, Vol. 45, pp. 91-98, 2012. [IF=0.904, Q4]
19) Aiman El-Maleh, Saif al Zahir and Esam Khan, "Test data compression based on geometric shapes," Computers & Electrical Engineering, Vol. 37, Issue 3, May 2011, Pages 376-391. [IF=1.747, Q2]
20) Esa Alghonaim, Aiman El-Maleh, M. Adnan Landolsi and Sadiq M. Sait, "A Platform for LDPC Code Design and Performance Evaluation," The Arabian Journal for Science and Engineering, Vol. 35, No. 2B, 2010, pp. 131-148. [IF=1.092, Q3]
21) Wenfa Zhan, Huaguo Liang, Cuiyun Jiang, Zhengfeng Huang, Aiman El-Maleh, "A scheme of test data compression based on coding of even bits marking and selective output inversion," Computers and Electrical Engineering 36 (2010), pp. 969-977. [IF=1.747, Q2]
22) Aiman El-Maleh, Bashir M. Al-Hashimi, Aissa Melouki and Farhan Khan, "Defect Tolerant N^2-Transistor Structure for Reliable Nanoelectronic Designs," IET Computers & Digital Techniques (Special Issue on Nanoelectronics), Vol. 3, Iss. 6, pp. 570-580, Nov. 2009. [IF=0.639, Q4]
23) Aiman El-Maleh, Mustafa I. Ali and Ahmad A. Al-Yamani, "Reconfigurable Broadcast Scan Compression Using Relaxation Based Test Vector Decomposition," IET Computers & Digital Techniques, Vol. 3, Iss. 2, pp. 143–161, March 2009. [IF=0.639, Q4]
24) Esa Alghonaim, Aiman El-Maleh and Adnan Al-Andalusi, "NEW TECHNIQUE FOR IMPROVING PERFORMANCE OF LDPC CODES IN THE PRESENCE OF TRAPPING SETS," EURASIP Journal on Wireless Communications and Networking, Article ID 362897, 12 pages, 2008. doi:10.1155/2008/362897 (A special issue on Advances in Error Control Coding Techniques). [IF=2.407, Q2]

25) Aiman El-Maleh, "Efficient Test Compression Technique Based on Block Merging," IET Comput. Digit. Tech., 2008, Vol. 2, No. 5, pp. 327–335. [IF=0.639, Q4]
26) Aiman El-Maleh, “Test Data Compression for System-on-a-Chip using Extended Frequency-Directed Run-Length (EFDR) Code,” IET Computers & Digital Techniques, 2008, Vol. 2, No. 3, pp. 155–163. [IF=0.639, Q4]
27) Aiman El-Maleh, Saqib Khurshid, “Efficient Test Compaction for Combinational Circuits Based on Fault Detection Count-Directed Clustering,” IET Computers & Digital Techniques, 2007, 1, (4), pp. 364–368. [IF=0.639, Q4]
28) Aiman El-Maleh, Saqib Khursheed, and Sadiq Sait, “Static Compaction Techniques for Sequential Circuits Based on Reverse Order Restoration and Test Relaxation” IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 25, NO. 11, NOVEMBER 2006, pp. 2556-2564. [IF=2.089, Q2]
29) Sadiq M. Sait, Aiman H. El-Maleh, and Raslan H Al-Abaji, “Evolutionary Algorithms for VLSI Multiobjective Netlist Partitioning,” ENGINEERING APPLICATIONS OF ARTIFICIAL INTELLIGENCE 19 (3), APR 2006, pp. 257-268. [IF=2.819, Q1]
30) Aiman El-Maleh, Sadiq Sait, and Syed Shazli, “Evolutionary Algorithms for State Justification in Sequential Automatic Test Pattern Generation,” ENGINEERING INTELLIGENT SYSTEMS FOR ELECTRICAL ENGINEERING AND COMMUNICATIONS 13 (1): 15-21, MAR 2005. [IF=0.205, Q4]
31) Aiman El-Maleh and Khaled Al-Utaibi, “An Efficient Test Relaxation Technique for Synchronous Sequential Circuits,” IEEE Transactions on Computer Aided Design of Integrated Circuits, Vol. 23, No. 6, pp. 933-940, June 2004. [IF=2.089, Q2]
32) Aiman El-Maleh and Yahya Osais, "Test Vector Decomposition Based Static Compaction Algorithms for Combinational Circuits", ACM Transactions on Design Automation of Electronic Systems, Volume 8, No. 4, pp. 430-459, October 2003. [IF=0.87, Q4]
33) Aiman El-Maleh, Thomas Marchok, Janusz Rajski, and Wojciech Maly, “Behavior and Testability Preservation Under the Retiming Transformation,” IEEE Transactions on Computer-Aided Desig, Vol. 16, pp. 528-543, May 1997. [[IF=2.089, Q2]
34) Thomas Marchok, Aiman El-Maleh, Wojciech Maly, and Janusz Rajski, “A Complexity Analysis of Sequential ATPG,” IEEE Transactions on Computer-Aided Design, Vol. 15, pp. 1409-1423, Nov. 1996. [IF=2.089, Q2]
35) Aiman El-Maleh and Janusz Rajski, “Delay Fault Testability Preservation of the Concurrent Decomposition and Factorization Transformations,” IEEE Transactions on Computer-Aided Design, Vol. 14, pp. 582-590, May 1995. (A special section on 12th IEEE VLSI Test Symposium.) [IF=2.089, Q2]
36) Thomas Marchok, Aiman El-Maleh, Janusz Rajski, and Wojciech Maly, “Testability Implications of Performance Driven Logic Synthesis,’’ in IEEE Design and Test of Computers, pp. 32-39, summer 1995.(A special issue on First International Test Synthesis Workshop.) [IF=1.623, Q2]
37) Sadiq M. Sait and Aiman H. El-Maleh, “State Machine Synthesis with Weinberger Arrays,” Int. Journal of Electronics, Vol. 71, No. 1, pp. 1-12, July 1991. [IF=0.939, Q4]

Refereed Conferences

1) Aiman H. El-Maleh, "A Sequential Circuit Fault Tolerance Technique with Enhanced Area and Power," 15th IEEE International Symposium on Signal Processing and Information Technology, pp. 301-304, 2015.
2) Aiman H. El-Maleh, "State Assignment for Power Optimization of Sequential Circuits based on a Probabilistic Pairwise Swap Search Algorithm," 15th IEEE International Symposium on Signal Processing and Information Technology, pp. 305-308, 2015.
3) Aiman H. El-Maleh, Feras Chikh Oughali, “Enhancing Reliability of Combinational Circuits against Soft Errors by Using a Generalized Modular Redundancy Scheme,” 2013 International Symposium on Electronic System Design, pp. 62-66.
4) Wenfa Zhan and Aiman H. El-Maleh, "A New Collaborative Scheme of Test Vector Compression Based on Equal-Run-Length Coding (ERLC)," The 13th International Conference on Computer Supported Cooperative Work in Design (CSCWD 2009), pp.21-25, April 2009.

5) Aiman H. El-Maleh, Bashir M. Al-Hashimi and Aissa Melouki, "Transistor-Level Based Defect-Tolerance for Reliable Nanoelectronics," The sixth ACS/IEEE International Conference on Computer Systems and Applications (AICCSA-08), Doha, Qatar, 2008 pp. 53-60.
6) Esa Al-Ghonaim, Aiman H. El-Maleh, and Adnan Andalusi, "Using input/output queues to increase LDPC decoder performance," The sixth ACS/IEEE International Conference on Computer Systems and Applications (AICCSA-08), Doha, Qatar, 2008, pp. 304-308.
7) Esa Alghonaim, Aiman El-Maleh and Adnan Al-Andalusi, " PARALLEL COMPUTING PLATFORM FOR EVALUATING LDPC CODES PERFORMANCE," IEEE International Conference on Signal Processing and Communications (ICSPC 2007), November 2007, Dubai, United Arab Emirates, pp. 157- 160.
8) Esa Alghonaim, Mohamed Adnan Landolsi, and Aiman El-Maleh, "IMPROVING BER PERFORMANCE OF LDPC CODES BASED ON INTERMEDIATE DECODING RESULTS," IEEE International Conference on Signal Processing and Communications (ICSPC 2007), November 2007, Dubai, United Arab Emirates, pp. 1547- 1550.
9) Aiman H. El-Maleh, Mustafa Imran Ali and Ahmad A. Al-Yamani, "A Reconfigurable Broadcast Scan Compression Scheme Using Relaxation Based Test Vector Decomposition," 16th IEEE Asian Test Symposium, Oct. 2007. pp. 91-94.
10) Aiman EL-MALEH, Bashir AL-HASHIMI, Ahmad AL-YAMANI, "Defect-Tolerant N^2-Transistor Structure for Reliable Design at the Nanoscale," IEEE European Test Symposium 2007, Freiburg, Germany.
11) Aiman El-Maleh, Saqib Khurshid, "Efficient Test Compaction for Combinational Circuits Based on Fault Detection Count-Directed Clustering," IEEE Int. Design and Test Workshop, Nov. 19-20, UAE, 2006.
12) Aiman El-Maleh, Basil Arkasosy, M. Adnan Al-Andalusi, "Interconnect-Efficient LDPC Code Design," 18th IEEE Int. Conf. on Microlelectronics, Dec. 2006, Dhahran, Saudi Arabia, pp. 127-130.
13) Aiman El-Maleh, "An Efficient Test Vector Compression Technique Based on Block Merging," IEEE Int. Symp. on Circuits and Systems, pp. 1447-1450, May 2006.
14) Aiman El-Maleh, Sadiq M. Sait and Faisal Nawaz Khan, "Finite State Machine State Assignment for Area and Power Minimization," IEEE Int. Symp. on Circuits and Systems, pp. 5303-5306, May 2006.
15) Aiman El-Maleh, Saqib Khursheed, and Sadiq Sait, "Static Compaction Techniques for Sequential Circuits Based on Reverse Order Restoration and Test Relaxation" IEEE 14th Asian Test Symposium, pp. 378 – 385, Dec. 18-21 2005.
16) Aiman El-Maleh and Yahya Osais, "A Class-based Clustering Static Compaction Technique for Combinational Circuits," The 16th International Conference on Microelectronics, pp. 522–525, 6-8 Dec. 2004.
17) Aiman El-Maleh and Yahya Osais, "On Test Vector Reordering for Combinational Circuits," The 16th International Conference on Microelectronics, pp. 772 – 775, 6-8 Dec. 2004.
18) Aiman El-Maleh, "A Hybrid Test Compression Technique for Efficient Testing of Systems-on-a-Chip," 10th IEEE International Conference on Electronics, Circuits and Systems, December 2003.
19) Yahya Osais and Aiman El-Maleh, "A Static Test Compaction Technique for Combinational Circuits Based on Independent Fault Clustering," 10th IEEE International Conference on Electronics, Circuits and Systems, December 2003.
20) Sadiq Sait, Aiman El-Maleh and Raslan Al-Abaji, "Enhancing Performance of Iterative Heuristics for VLSI Netlist Partitioning", 10th IEEE International Conference on Electronics, Circuits and Systems, December 2003.
21) Aiman El-Maleh and Khaled Al-Utaibi, "An Efficient Test Relaxation Technique for Synchronous Sequential Circuits" Proc. of the 21'th IEEE VLSI Test Symposium (VTS), pp. 179-185, 2003.
22) Aiman El-Maleh and Khaled Al-Utaibi, " ON EFFICIENT EXTRACTION OF PARTIALLY SPECIFIED TEST SETS FOR SYNCHRONOUS SEQUENTIAL CIRCUITS " Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS), pp. V-545 - V-548, 2003.
23) Sadiq Sait, Aiman El-Maleh and Raslan Al-Abaji, "SIMULATED EVOLUTION ALGORITHM FOR MULTIOBJECTIVE VLSI NETLIST BI-PARTITIONING" Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS), pp. V-457 - V-460, 2003.
24) Sadiq Sait, Aiman El-Maleh and Raslan Al-Abaji, "GENERAL ITERATIVE HEURISTICS FOR VLSI MULTIOBJECTIVE PARTITIONING" Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS), pp. V-497 - V-500, 2003.

25) Aiman El-Maleh and Ali Al-Suwaiyan, "An Efficient Test Relaxation Technique for Combinational and Full-Scan Sequential Circuits" Proc. of the 20'th IEEE VLSI Test Symposium (VTS), pp. 53-59, 2002.
26) Aiman El-Maleh and Ali Al-Suwaiyan, "An Efficient Test Relaxation Technique for Combinational Circuits Based on Critical Path Tracing" Proc. of the 9th IEEE International Conference on Electronics, Circuits and Systems, pp. 461-465, Sep. 2002.
27) Aiman El-Maleh and Raslan Al-Abaji, "Extended Frequency-Directed Run Length Code with Improved Application to System-on-a-chip Test Data Compression" Proc. of the 9th IEEE International Conference on Electronics, Circuits and Systems, pp. 449-452, Sep. 2002.
28) Aiman El-Maleh and Ali Al-Suwaiyan, "An Efficient Test Relaxation Technique for Combinational Logic Circuits", Proc. of the Six'th Saudi Engineering Conference, Vol. 4, pp. 155-165, Dec. 2002.
29) Aiman El-Maleh and Raslan Al-Abaji, "On Improving the Effectiveness of System-on-a-Chip Test Data Compression based on Extended Frequency-Directed Run Length Codes" Proc. of Six'th Saudi Engineering Conference, Vol. 4, pp. 145-153, Dec. 2002.
30) Sadiq Sait, Aiman El-Maleh and Raslan Al-Abaji, "Evolutionary Heuristics for Multiobjective VLSI Nestlist Bi-Partitioning" Proc. of Six'th Saudi Engineering Conference, Vol. 4, pp. 131-143, Dec. 2002.
31) Aiman El-Maleh, Saif Al-Zahir, and Esam Khan,"A Geometric-Primitives-Based Compression Scheme for Testing Systems-on-a-Chip," 19'th IEEE VLSI Test Symposium (VTS), pp. 54-59, 2001.
32) Aiman El-Maleh, and Yahya Osais,"A Retiming-Based Test Pattern Generator Design for Built-In Self Test of Data Path Architectures," Int. Symp. on Circuits and Systems (ISCAS), pp. 550-553, 2001.
33) Aiman El-Maleh, Sadiq Sait, and Syed Shazli,"An Iterative Heuristic for State Justification in Sequential Automatic Test Pattern Generation," 2001 Genetic and Evolutionary Computation Conference (GECCO).
34) Aiman El-Maleh, Sadiq Sait, and Syed Shazli,"An Evolutionary Meta-Heuristic for State Justification in Sequential Automatic Test Pattern Generation," International Joint INNS-IEEE Conference on Neural Networks (IJCNN), pp. 767-772, 2001.
35) Saif Al-Zahir, Aiman El-Maleh, and Esam Khan, "An Efficient Test Vector Compression Technique Based on Geometric Shapes," the 8th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2001), pp. 1561-1564, 2001.
36) Sadiq Sait, Habib Yousef, Aiman El-Maleh, and Mahmud Minhas, "Iterative Heuristics for Multiobjective VLSI Standard Placement", International Joint INNS-IEEE Conference on Neural Networks (IJCNN), pp. 2224-2229, 2001.
37) Sadiq Sait, Habib Yousef, Junaid Khan, and Aiman El-Maleh, "Fuzzy Simulated Evolution for Low power and High Performance Optimization of VLSI Placement", International Joint INNS-IEEE Conference on Neural Networks (IJCNN), pp. 738-743, 2001.
38) Sadiq Sait, Habib Yousef, Junaid Khan, and Aiman El-Maleh, "Fuzzified Iterative Algorithms for Performance Driven Low Power VLSI Placement", International Conference on Computer Design (ICCD), pp. 484-487, 2001.
39) Aiman El-Maleh, Mark Kassab, and Janusz Rajski,"A Fast Sequential Learning Technique for Real Sequential Circuits with Application to Enhancing ATPG Performance," in Proc. of 32nd Design Automation Conference , pp. 625-631, June 1998.
40) Wu-Tung Cheng, Aiman El-Maleh, Rob Thompson, Don Ross, and Janusz Rajski, "The Pitfalls of Necessary Assignments", Fourth International Test Synthesis Workshop, May 1997, Santa Barbara, CA.
41) Janusz Rajski, Aiman El-Maleh, and Jerzy Tyszer, "Arithmetic BIST Tackles Embedded Cores," Electronic Engineering Times, Oct. 21, 1996.
42) Aiman El-Maleh, Thomas Marchok, Janusz Rajski, and Wojciech Maly, "On Test Set Preservation of Retimed Circuits," in Proc. of the 32nd Design Automation Conference, pp. 176-182, June 1995.(Best paper award nomination.)
43) Thomas Marchok, Aiman El-Maleh, Wojciech Maly, and Janusz Rajski, "Complexity of Sequential ATPG," in Proc. of the European Design and Test Conference, pp. 252-261, March 1995 (Winner of the best paper award for the most outstanding contribution in the field of test in 1995).
44) Aiman El-Maleh and Janusz Rajski, "Algebraic Resubstitution with Complement and Testability Preservation," Presented at the First International Test Synthesis Workshop, May 1994, Santa Barbara, CA.

45) Thomas Marchok, Aiman El-Maleh, Wojciech Maly, and Janusz Rajski, “Test Set Preservation under Retiming Transformation,”Presented at the First International Test Synthesis Workshop, May 1994, Santa Barbara, CA.
46) Aiman El-Maleh and Janusz Rajski, “Delay-Fault Testability Preservation of the Concurrent Decomposition and Factorization Transformations,” in Proc. of IEEE VLSI Test Symposium, April 1994, pp. 15-21.
47) Janusz Rajski, Jagadeesh Vasudevamurthy, and Aiman El-Maleh, “Recent Advances in Logic Synthesis with Testability,” in Proc. of IEEE VLSI Test Symposium, April 1992, pp. 254-256.
48) Aiman H. El-Maleh, Fayez El-Guibaly, and V.K. Bhargava, “Improving the Performance of One-Dimensional Vector Quantization Using Product Structures,” in Proc. of the 1991 First Cyprus International Conference on Computer Applications to Engineering Systems, Nicosia, Cyprus, July 1991, pp. 40-45.
49) Aiman H. El-Maleh, Fayez El-Guibaly, and V.K. Bhargava, “A Comparison of One- And Two-Dimensional Vector Quantization of Images,” in Proc. of the 1991 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, Victoria, Canada, Vol. 2, May 1991, pp. 490-493.
50) Aiman H. El-Maleh and Sadiq M. Sait, “A State Machine Synthesizer With Weinberger Arrays,” in Proc. of the 1991 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, Victoria, Canada, Vol. 2, May 1991, 753-756.

Book Chapters

Aiman H. El-Maleh, Bashir M. Al-Hashimi, Aissa Melouki, and Ahmad Al-Yamani, “Transistor-Level Based Defect-Tolerance for Reliable Nanoelectronics,” pp. 29-50, Robust Computing with Nano-scale Devices: Progresses and Challenges, Chao Huang, Springer, ISBN 978-90-481-8539-9, 2010.

Patents

1. *Aiman H. El-Maleh, “Systems and Method for Optimizing State Encoding," US Patent 10042965, August 2018.*
2. *Aiman H. El-Maleh and Ahmad T. Sheikh, “Method of Fault Tolerance in Combinational Circuits," US Patent 10013296, July. 2018.*
3. *Aiman H. El-Maleh and Feras Chikh Oughali, “Generalized Modular Redundancy Fault Tolerance Method for Combinational Circuits,” US Patent 9,075,111, July 2015.*
4. *Aiman H. El-Maleh and Khaled Daud, “Method for Synthesizing Soft Error Tolerant Combinational Circuits,” US Patent 8,640,063, Jan. 2014.*
5. *Aiman H. El-Maleh, Wojciech Maly, Thomas E. Marchok, Janusz Rajski, “Test Pattern Generation for an Electronic Circuit Using a Transformed Circuit Description,” US Patent 5,528,604, June 1996.*

Thesis Supervision

1. Ahmad Tariq Sheikh, "AN INTEGRATED APPROACH FOR SOFT ERROR TOLERANCE OF COMBINATIONAL CIRCUITS," PhD, April 2016 (Supervisor).
2. Feras Chickh Oughali, A Generalized Modular Redundancy Scheme for Enhancing Fault Tolerance of Combinational Circuits, M.Sc., Oct. 2012 (Supervisor).
3. Khaled Abdul Karim Daud, Synthesis of Soft-Error Tolerant Combinational Circuits, M.Sc., April 2012 (Supervisor).
4. Ayed Saad Al-Qahtani, Fault Tolerance Techniques for Sequential Circuits: A Design Level Approach, M.Sc., June 2010 (Supervisor).
5. Ahmad Al-Masry, DESIGN FOR DEFECT TOLERANT RELIABLE DIGITAL SYSTEMS AT THE NANOSCALE, M.Sc., June 2009 (Supervisor).
6. Farhan Khan, TRANSISTOR-LEVEL DEFECT-TOLERANT TECHNIQUES FOR RELIABLE DESIGN AT THE NAOSCALE, M.Sc., June 2009 (Supervisor).

7. Badr Hamad Al-Dohan, Implementation of Low Density Parity-Check Codes for Wireless Communications, M.Sc., May 2008. (Co-supervisor).
8. Esa Al-Ghonaim, LDPC Codes Design and Decoder Implementation, PhD, Feb. 2008 (Supervisor).
9. Mustafa Imran Ali, An Efficient Relaxation-based Test width compression technique for multiple scan chain testing, M.Sc., Sep. 2006 (Supervisor).
10. Faisal Nawaz Khan, Finite State Machine Encoding/State Assignment for Low Power, Reduced Area and Increased Testability using Iterative Algorithms, M.Sc., June 2005 (Supervisor).
11. Syed Saqib Khursheed, Test Set Compaction for Sequential Circuits based on Test Relaxation, M.Sc., Dec. 2004 (Supervisor).
12. Yahya I. Osais, Efficient Static Compaction Algorithms for Combinational Circuits Based on Test Relaxation, M.Sc., Oct. 2003 (Supervisor).
13. Raslan Al-Abaji, Evolutionary Techniques for Multi-Objective VLSI Netlist Partitioning, M .Sc., May 2002 (Co-supervisor).
14. Khaled Al-Utaibi, An Efficient Test Relaxation Technique for Sequential Circuits,M.Sc., May 2002 (Supervisor).
15. Ali Al-Suwaiyan, An Efficient Test Vector Relaxation Technique for Combinational Circuits, M.Sc., May 2002 (Supervisor).
16. Esam Khan, A Two-Dimensional Geometric-Primitives-Based Compression Scheme for Testing Systems-on-a-Chip, M.Sc., May 2001(Supervisor).
17. Syed Zafar Shazli, Experimenting with Iterative Heuristics for State Justification in Sequential ATPG, M.Sc., Apr. 2001 (Supervisor).

Teaching Experience

Undergraduate Courses:

1. ICS 103 Computer Programming in C
2. EE 200 Digital Logic Circuit Design
3. COE 202 Digital Logic Design
4. COE 203 Digital Logic Laboratory
5. COE 205 Computer Organization & Assembly Language
6. ICS 233 Computer Architecture & Assembly Language
7. COE 301 Computer Organization
8. COE 306 Introduction to Embedded Systems
9. COE 308 Computer Architecture
10. ISE 307 Engineering Economic Analysis
11. COE 342 Data & Computer Communication
12. COE 360 Principles of VLSI Design
13. COE 390 Seminar
14. COE 405 Design & Modeling of Digital Systems
15. COE 464 Testing of Digital Circuits

Graduate Courses:

1. COE 561 Digital System Design & Synthesis
2. COE 571 Digital System Testing