Defect-Tolerant N^2-Transistor Structure for Reliable Design at the Nanoscale

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ABSTRACT

Nanodevices based circuit design will be based on the acceptance that a certain percentage of devices in the design will be defective. In this work, we investigate a defect-tolerant technique that adds redundancy at the transistor level and provides built-in immunity to permanent defects. The investigated technique is based on replacing each transistor by an N^2-transistor structure (N=2, 3,..k). An N^2-transistor structure guarantees defect tolerance of all defects of multiplicity ≤ (N-1) in each transistor structure. Thus, a large number of multiple defects, distributed among the structures, can be tolerated. We provide a theoretical analysis of circuit probability of failure and reliability that matches experimental results. As demonstrated by extensive experimental results, the investigated technique achieves significantly higher defect tolerance than classical gate-level defect-tolerant techniques such as Triple Modular Redundancy (TMR) and quadded logic (higher defect tolerance with even 4 to 5 times more transistor defect probability). Furthermore, it requires nearly half the transistor count of the quadded logic technique.

1. INTRODUCTION

Recent advances in emerging nanotechnologies enabled researchers to successfully build logic gates and memory arrays [1-4]. Nanodevices such as carbon nanotubes hold the promise of increased integration densities and reduced power consumption for future non-silicon electronic circuits. It is expected and experimentally shown, however, that nanodevices will suffer from significantly increased permanent failure rates mainly due to the fundamental limitations of the fabrication processes that limit the yield of such devices [3-5]. At these nanometer scales, the small cross section areas of wires make them fragile, increasing the likelihood that they will break during assembly. Moreover, the contact area between nanowires, and between nanowires and devices depends on a few atomic-scale bonds resulting in some connections being poor and effectively unusable [3, 6, 7]. Therefore, the necessity to cope with intrinsic defects at the circuit level must be recognized as a key aspect of nanodevices-based designs. To implement such robustness and defect tolerance, circuit design techniques capable of absorbing a number of defects and still be able to perform their functions need to be investigated.

Typical approaches to reliable system design include defect-tolerant and defect-avoidance techniques [8]. Defect-tolerant techniques are based on adding redundancy in the design to tolerate defects or faults. However, defect-avoidance techniques are based on reconfigurable blocks. Examples of defect-tolerant techniques are [9, 10, 13, 14, 15]. Examples of defect-avoidance techniques are [5, 7, 8, 16-18].

While both approaches address the defect-tolerance issue, it is unclear from the literature which approach is more effective since defect-tolerant approaches require extensive redundancy addition, whilst defect-avoidance techniques require extensive defect mapping and reconfiguration infrastructure.

To tolerate defects, redundancy can be added at the transistor level, gate level or functional block level. In this work, we evaluate a defect-tolerant technique based on redundancy addition at the transistor level. We compare this approach with techniques based on redundancy addition at the gate level. We provide theoretical analysis for circuit failure probability and reliability of the evaluated technique. The theoretical expressions derived are validated by experimental results.

2. PREVIOUS APPROACHES

The multiplexed logic approach, motivated by the pioneering work of John von Neumann [9], began as an attempt to build early digital computers out of unreliable components. This approach and subsequent derivatives [10-12] have provided insight on how to design reliable nanoelectronic systems out of components that might fundamentally be less reliable than those of currently available technologies. In the multiplexed logic approach, each logic gate is duplicated N times and each input and output is also duplicated N times. The inputs randomly pair to feed the N gates. The logic state of the bundle of N wires is decided based on the fraction of wires having a specific value above or below a preset threshold. In general, von Neumann's construction requires a large amount of

redundancy and a low error rate for individual gates. Another defect-tolerant approach is known as the N-tuple modular redundancy (NMR) in which each gate is duplicated N times (where N must be an odd number) followed by an arbitration unit deciding the correct value based on majority. Triple-modular redundancy (TMR) is a special case of NMR. The reliability of such designs is limited by that of the final arbitration unit, making the approach difficult in the context of highly integrated nanosystems [8]. A TMR circuit can be further triplicated. The obtained circuit thus has nine copies of the original module and two layers of majority gates. This process can be repeated if necessary, resulting in a technique called cascaded triple modular redundancy (CTMR) or recursive triple modular redundancy (RTMR). Spagocci and Fountain [14] have shown that using CTMR in a nanochip with large nanoscale devices would require an extremely low device error rate. In [15], it is shown that recursive voting leads to a double exponential decrease in a circuit's failure probability. However, a single error in the last majority gate can cause an incorrect result, hampering the technique's effectiveness. Pierce [10] introduced a fault-tolerant technique called interwoven redundant logic. Quadded logic [11-13] is an ad hoc configuration of the interwoven redundant logic. It requires four times as many circuits. A quadded circuit implementation based on NAND gates replaces each NAND gate with a group of four NAND gates, each of which has twice as many inputs as the one it replaces. While quadded logic guarantees tolerance of most single errors, errors occurring at the last two stages of logic may not be corrected. Figure 1 shows an example of TMR and quadded logic circuits.

Moore et al. [21] have analyzed the use of series-parallel and bridge configurations for the application of redundancy to relay networks. Suran [22] has evaluated the reliability of the quad-relay structure shown in Figure 2(b) and has shown its application using bipolar junction transistors. However, only the reliability of a single structure is evaluated and no extensive circuit reliability analysis is made. In this work, we evaluate defect tolerance based on adding redundancy at the transistor-level for CMOS circuits. We investigate circuit reliability based on the quadded structure in [22] more thoroughly and generalize it. Furthermore, a comparison is made with recent approaches proposed for defect tolerance in nanoelectronics.

3. TRANSISTOR-LEVEL BASED DEFECT TOLERANCE

In order to tolerate single-defective transistors, each transistor, A, is replaced by a quadded-transistor structure implementing either the logic function (A+A)(A+A) or the logic function (AA)+(AA), as shown in Figure 2. In both of the quadded-transistor structures shown in Figure 2 (b) & (c), any single transistor defect (stuck-open or stuck-short)

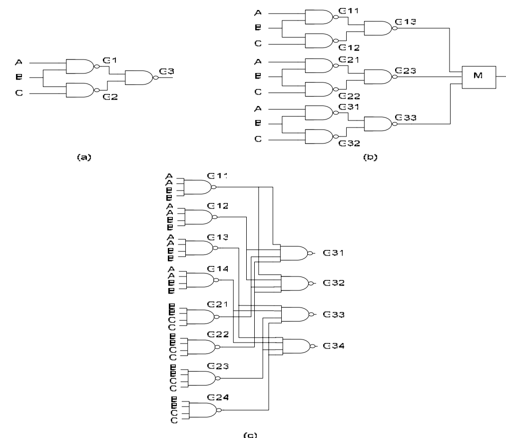

Figure 1 (a) Original circuit, (b) TMR circuit, (c) Quadded logic circuit.

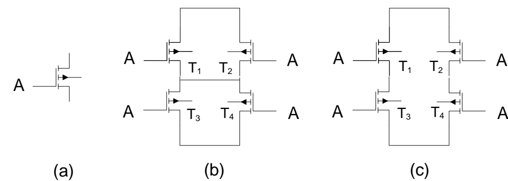

Figure 2 (a) Transistor in original gate implementation, (b) First quadded-transistor structure, (c) Seconed quadded-transistor structure.

will not change the logic behavior, and hence the defect is tolerated. Furthermore, double stuck-open defects are tolerated as long as they do not occur in any two parallel transistors (T_1&T_2 or T_3&T_4 for the structure in Figure 2(b), and T_1&T_2, T_1&T_4, T_3&T_2 or T_3&T_4 for the structure in Figure 2(c)). Double stuck-short defects are tolerated as long as they do not occur in any two series transistors (T_1&T_3, T_1&T_4, T_2&T_3 or T_2&T_4 for the structure in Figure 2(b), and T_1&T_3 or T_2&T_4 for the structure in Figure 2(c)). In addition, any triple defect that does not include two parallel stuck-open transistors or two series stuck-short transistors is tolerated. Thus, one can easily see that using either of the quadded-transistor structures, the reliability of gate implementation is significantly improved. It should be observed that the effective resistance of the quadded-transistor structures has the same resistance as the original transistor. However, in the presence of a single defect, the worst case effective resistance of the first quadded-transistor structure (Figure 2(b)) is 1.5R while that of the second quadded-transistor structure (Figure 2(c)) is 2R, where R is the effective resistance of a transistor. This occurs in the case of single stuck-open defects. For tolerable multiple defects, the worst case effective resistance of both structures is 2R. For this reason, the first quadded-transistor structure (Figure 2(b)) is adopted in this work.

Next, we determine the probability of circuit failure given a transistor defect probability using quadded-transistor

structures. A transistor is considered defective if it does not function properly either due to manufacturing defects or due to errors occurring during circuit operation.

Theorem 1[1]**:** *Given a transistor-defect probability, P, the probability of quadded-transistor structure failure is* $P_q = \frac{3}{2}P^2 - \frac{1}{2}P^3$

Proof: If there are only two defective transistors in a quadded-transistor structure, then we have four possible pairs of stuck-open and stuck short defects. In all cases, only one of those pair of defects produces an error. Thus, the probability of failure in this case is $\frac{1}{4} * \binom{4}{2} P^2 (1-P)^2 = \frac{3}{2} P^2 (1-P)^2$

If we assume that three transistors are defective, then we have eight possible combinations of stuck-open and stuck short defects. In all cases, five out of those combinations produce an error. Thus, the probability of failure in this case is

$$\frac{5}{8} * \binom{4}{3} P^3 (1-P) = \frac{5}{2} P^3 (1-P)$$

If four transistors are assumed defective, then in this case there will always be an error and the probability of failure is

$$1 * \binom{4}{4} P^4 = P^4$$

Thus, the probability of quadded-transistor structure failure is

$$P_q = \frac{3}{2}P^2(1-P)^2 + \frac{5}{2}P^3(1-P) + P^4$$
$$= \frac{3}{2}P^2 - 3P^3 + \frac{3}{2}P^4 + \frac{5}{2}P^3 - \frac{5}{2}P^4 + P^4$$
$$= \frac{3}{2}P^2 - \frac{1}{2}P^3$$ ■

Theorem 2: *Given a transistor-defect probability, P, and a circuit with N quadded-transistor structures, the probability of circuit failure is*

$$P_f = \sum_{i=1}^{N} (-1)^{i+1} \binom{N}{i} (P_q)^i$$

Corollary 1: *Given a transistor-defect probability, P, and a circuit with N quadded-transistor structures, the circuit reliability* $R = 1 - P_f = 1 - \sum_{i=1}^{N} (-1)^{i+1} \binom{N}{i} (P_q)^i$.

We assume in this work that circuit reliability represents the probability that the circuit will function correctly in the presence of defects. Figure 3 compares the reliability of several NAND gates of various inputs, 2 to 8, implemented using the quadded-transistor structure and conventional complementary (pull-up, pull-down) CMOS implementation. As can be seen, the reliability of gates implemented using the quadded-transistor structure is significantly higher than the reliability of conventional gate implementation. For example, for an 8-input NAND gate, with a probability of transistor failure = 10%, the probability of failure for the quadded-transistor structure-based design is 21% (and reliability is 79%), while the probability of failure for the conventional CMOS implementation is 81% (and reliability is 19%). Furthermore, as the number of inputs increases, the probability of gate failure increases and reliability decreases, as expected.

The quadded-transistor structure, given in Figure 2(b), can be generalized to an N^2-transistor structure, where N=2, 3,…, k. An N^2-transistor structure is composed of N blocks connected in series with each block composed of N parallel transistors, as shown in Figure 4. An N^2-transistor structure guarantees defect tolerance of all defects of multiplicity less than or equal to (N-1) in the structure. Hence, a large number of multiple defects can be tolerated in a circuit implemented based on these structures. Furthermore, it can be shown that the probability of failure for an N^2-transistor structure is $O(P^N)$ assuming a transistor-defect probability, *P* (not included due to space limitation).

An interesting advantage of the N^2-transistor structures is that that they fit well in existing design and test methodologies. In synthesis, a library of gates implemented based on the quadded-transistor structure will be used in the technology mapping process. The same testing methodology

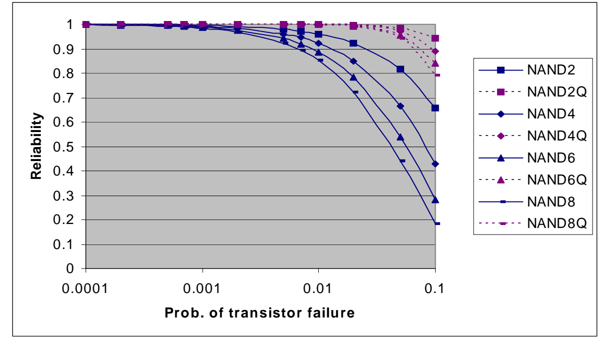

Figure 3 Gate reliability comparison between quadded-transistor structure (Q) and complementary CMOS .

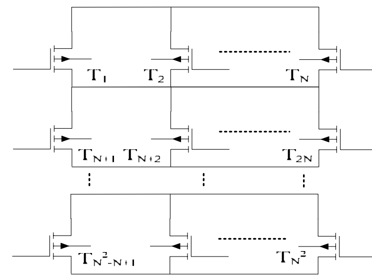

Figure 4 Defect-tolerant N^2-transistor structure.

[1] A similar result is given in [22] expressed as the probability of correct operation of a quadded structure given the probability of correct operation of a relay.

Table 1. **Area, delay and power values of basic 0.5µ cells designed using quadded-transistor structure (Fig. 2b) and complementary (pull-up, pull-down) CMOS.**

Characteristics		INV		NAND2		NOR2	
		CMOS	QT	CMOS	QT	CMOS	QT
Delay (ps)	Fall	270.8	763.0	416.6	1143	285.7	902.5
	Rise	566.6	1775	606.9	2217	1124	3986
	T_{PHL}	169.6	469.0	239.1	604.9	180.7	557.6
	T_{PLH}	300.3	973.3	324.9	1182	548.2	1965
Dyn. Power (mW)	Avg.	0.120	0.340	0.175	0.533	0.180	0.542
	Max.	1.469	2.602	1.709	2.602	1.691	2.606
	RMS	0.355	0.665	0.431	0.815	0.432	0.810
Area (um^2)		89	208	128	402	126	397

will be used assuming testing is done at the gate level based on the single stuck-at fault model. So, the same test set derived for the original gate-level structure can be used without any change.

The gate capacitance that the quadded-transistor structure induces on the gate connected to the input A is four times the original gate capacitance. This has an impact on both delay and power dissipation. However, as shown in [19], a gate with higher load capacitance has better noise rejection curves and hence is more resistant to soft errors resulting in noise glitches. To determine the area, delay and power impact of the quadded-transistor structure, we have designed, using Magic, two libraries based on the 0.5u CMOS Alcatel process. The libraries are composed of three basic cells, Inverter (INV), 2-input Nand gate (NAND2), and 2-input Nor gate (NOR2) based on the quadded-transistor structure and the conventional CMOS implementation. Then, we obtained delay and power characteristics using SPICE simulations based on the extracted netlists. Delay characteristics were calculated after supplying proper load and drive conditions. For all the cells the drive was composed of two inverters in series and the load was composed of two inverters in parallel. The inverters were chosen from the same library. Dynamic power was measured using the .measure command in SPICE for the same period of time in both libraries. Table 1 summarizes delay, power and area characteristics of the two libraries. The delay and power consumption of cells designed based on the quadded-transistor structure are in the worst case 3.65 times more than the conventional cells and the cell area is about 3 times more. As with all defect-tolerant techniques, the increase in area, power and delay is traded off by more circuit reliability. This is justified given that nanotechnology will provide much higher integration densities, speed and power advantages.

In order to tolerate defects in interconnects, we propose that four parallel interconnect lines are used to connect the driving gate to the four transistors in a quadded-transistor structure. This guarantees tolerance of any single interconnect defect. This also results in a faster charging of the load capacitance and hence may improve the delay.

4. EXPERIMENTAL RESULTS

To demonstrate the effectiveness of the quaded-transistor structure technique, we have performed experiments on a number of the largest ISCAS85 and ISCAS89 benchmark circuits (replacing flip-flops by inputs and outputs).

For evaluating circuit failure probability and reliability, we adopt the simulation-based reliability model used in [13]. We compare circuit reliability based on the quadded-transistor structure with the compared approaches in [13] including Triple Interwoven Redundancy (TIR) and Quadded logic. We assume a defect model of having a transistor either stuck-open or stuck-short. We use a complete test set T that detects all detectable single stuck-at faults in a circuit. We have used test sets generated by Mintest ATPG tool [20]. To compute the circuit failure probability, F_m, resulting from injecting m defective transistors, we use the following procedure:

1. Set the number of iterations to be performed, I, to 1000 and the number of failed simulations, K, to 0.
2. Simulate the fault-free circuit by applying the test set T.
3. Randomly inject m transistor defects.
4. Simulate the faulty circuit by applying the test set T.
5. If the outputs of the fault-free and faulty circuits are different, increment K by 1.
6. Decrement I by 1 and if I is not 0 goto step 3.
7. Failure Rate $F_m = K/1000$.

Assuming that every transistor has the same defect probability, P, and that defects are randomly and independently distributed, the probability of having a number of m defective transistors in a circuit with N transistors follows the binomial distribution [13] as shown below:

$$P(m) = \binom{N}{m} P^m \times (1-P)^{N-m}$$

Assuming the number of transistor defects, m, as a random variable and using the circuit failure probability F_m as a failure distribution in m, the probability of circuit failure, F, and circuit reliability, R, are computed as follows [13]:

$$F = \sum_{m=0}^{N} F_m \times P(m)$$

$$R = 1 - F = 1 - \sum_{m=0}^{N} F_m \times P(m)$$

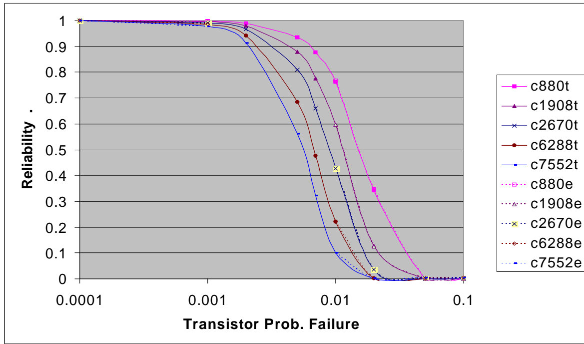

Figure 5 Reliability obtained both theoretically (t) and experimentally (e) based on quadded-transistor structure.

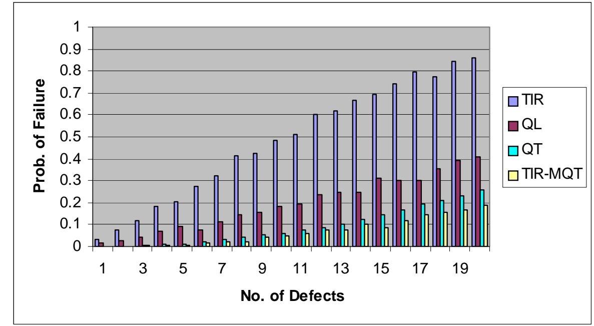

Figure 6 Comparison of circuit failure probability for an 8-stage cascaded half-adder circuit.

Figure 5 shows the reliability of some of the ISCAS85 benchmark circuits obtained both theoretically (based on Theorem 1&2) and experimentally based on the above simulation procedure and formulas. As can be seen, there is almost identical match, clearly validating the derived theoretical results.

In Figure 6, we compare the probability of circuit failure for a given number of defects between the quadded-transistor structure (QT), quadded logic (QL) [12, 13] and TIR logic [13]. It should be observed that TIR is a generalization of TMR logic. The comparison is made based on an 8-stage cascaded half adder circuit used in [13]. TIR logic is implemented by adding a majority gate for each sum and carry-out signal at each stage. Majority gate is also implemented as a single gate. As can be seen, the probability of circuit failure obtained by the quadded-transistor structure implementation is significantly better than those obtained by the TIR logic and quadded logic. This is in addition to the smaller number of transistors used. The number of transistors in the quadded-transistor structure implementation is 512, while it is 608 in TIR logic and 1024 in quadded logic. It should be observed that the total number of transistors in the circuit should be taken into account when making the comparison for a given number of defects as the percentage of injected defects varies.

The probability of circuit failure for TIR and TMR logic can be significantly improved by improving the reliability of majority gates. We have implemented the majority gates in the 8-stage cascaded half adder TIR logic circuit based on the quadded-transistor structure (TIR-MQT). As shown in Figure 6, the reliability of the implemented circuit is significantly improved compared to TIR circuit at the expense of increased number of transistors (No. transistors=1280). This shows an interesting potential application of the N^2-transistor structure in improving the reliability of voter-based redundancy techniques that will be more thoroughly investigated in future work.

For TMR to be effective, a careful balance between the module size and the number of majority gates used needs to be made. For this reason, we focus comparison of the reliability of ISCAS benchmark circuits between quadded-transistor structure and quadded logic.

A comprehensive comparison of the probability of circuit failure between the quadded-transistor structure and the quadded logic is given in Table 2 for several percentages of injected defects. For all the circuits, the quadded-transistor technique achieves significantly lower circuit failure probability than the quadded logic technique for the same and for twice the percentage of injected defects. For 10 out of 12 circuits, it achieves lower failure probability with four times the percentage of injected defects. In Table 3, we report the reliability results obtained based on the simulation procedure outlined above for the quadded-transistor structure and quadded logic approaches for several transistor defect probabilities. The effectiveness of the quadded-transistor structure technique is clearly demonstrated by the results as it achieves higher circuit reliability with even 4 to 5 times more transistor defect probability. This is in addition to the observation that it requires nearly half the area of quadded logic as indicated by the number of transistors.

5. CONCLUSION

In this work, we have investigated a transistor-level defect-tolerant technique based on replacing each transistor by an N^2-transistor structure (N=2, 3,…,k). An N^2-transistor structure guarantees defect tolerance of all defects of multiplicity $\leq$ (N-1) in each structure. We have provided both a theoretical and experimental analysis for the quadded-transistor structure, with N=2. Experimental results have demonstrated that the quadded-transistor structure provides significantly less circuit failure probability and higher reliability with nearly half the required area of quadded logic defect tolerant technique. It is also significantly better than Triple-Modular Redundancy and Triple Interwoven Redundancy defect-tolerant techniques. Unlike TIR and TMR which are limited by not tolerating defects occurring in majority gates, and quadded logic which may not tolerate defects occurring at the last two stages of gates in the design, the quadded-transistor structure tolerates possible defects distributed equally likely in the design. The defect tolerance effectiveness of the quadded-transistor

Circuit	Quadded-Transistor Structure					Quadded Logic				
	#Trans.	0.25%	0.5%	0.75%	1%	#Trans.	0.25%	0.5%	0.75%	1%
c880	7208	0.015	0.060	0.135	0.237	13616	0.452	0.783	0.905	0.978
c1355	9232	0.023	0.082	0.176	0.287	18304	0.531	0.846	0.975	0.995
c1908	13784	0.030	0.115	0.248	0.400	24112	0.673	0.94	0.984	1
c2670	22672	0.047	0.188	0.375	0.569	36064	0.958	0.999	1	1
c3540	30016	0.067	0.238	0.457	0.674	46976	0.59	0.901	0.996	0.999
c5315	45048	0.095	0.341	0.614	0.816	74112	0.991	1	1	1
c6288	40448	0.085	0.307	0.576	0.787	77312	0.685	0.962	0.999	1
c7552	61600	0.136	0.441	0.732	0.909	96816	0.985	1	1	1
s5378	35608	0.081	0.282	0.521	0.737	59760	1	1	1	1
s9234	74856	0.166	0.510	0.791	0.939	103488	0.999	1	1	1
s13207	103544	0.212	0.625	0.888	0.980	150448	1	1	1	1
s15850	128016	0.257	0.697	0.936	0.992	171664	1	1	1	1

Table 3. **Comparison of circuit reliability between quaded-transistor structure and quadded logic approaches.**

Circuit	Quadded-Transistor Structure						Quadded Logic					
	#Trans.	0.0001	0.001	0.002	0.005	0.01	#Trans.	0.0001	0.001	0.002	0.005	0.01
c880	7208	0.999	0.997	0.989	0.934	0.767	13616	0.979	0.822	0.651	0.283	0.042
c1355	9232	0.999	0.996	0.986	0.917	0.713	18304	0.975	0.765	0.575	0.187	0.008
c1908	13784	0.999	0.994	0.979	0.879	0.596	24112	0.975	0.755	0.558	0.261	0.001
c2670	22672	0.999	0.991	0.967	0.809	0.427	36064	0.904	0.350	0.112	0.001	0.000
c3540	30016	0.999	0.989	0.956	0.755	0.327	46976	0.981	0.805	0.614	0.237	0.000
c5315	45048	0.999	0.984	0.935	0.656	0.185	74112	0.853	0.227	0.034	0.001	0.000
c6288	40448	0.999	0.986	0.941	0.685	0.222	77312	0.971	0.718	0.465	0.024	0.000
c7552	61600	0.999	0.978	0.912	0.562	0.101	96816	0.874	0.292	0.077	0.000	0.000
s5378	35608	0.999	0.985	0.948	0.717	0.263	59760	0.811	0.134	0.015	0.001	0.000
s9234	74856	0.999	0.972	0.894	0.496	0.061	103488	0.821	0.140	0.001	0.000	0.000
s13207	103544	0.999	0.961	0.856	0.379	0.023	150448	0.518	0.008	0.000	0.000	0.000
s15850	128016	0.999	0.953	0.825	0.302	0.008	171664	0.576	0.009	0.000	0.000	0.000

technique merits further investigation in evaluating the structure performance in dealing with other defect models including bridging faults, which is future work.

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