Name: KEY Id#

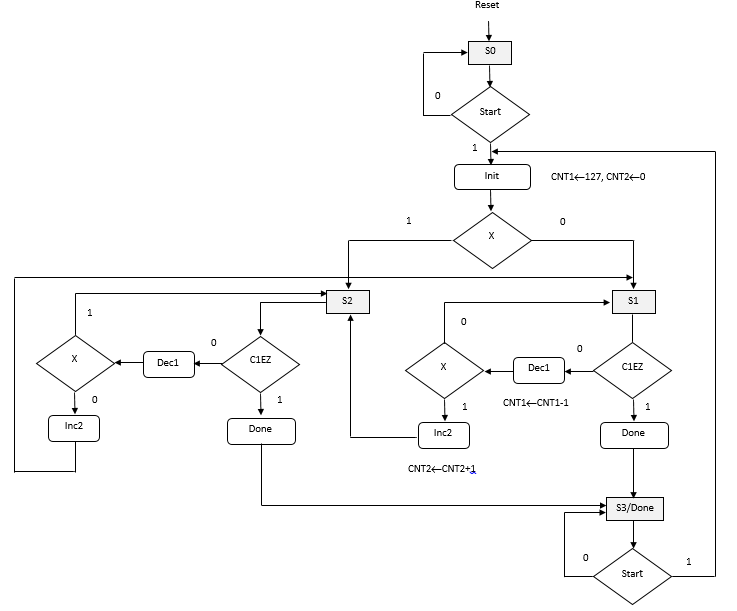
COE 405, Term 152

Design & Modeling of Digital Systems

Quiz# 5

Date: Sunday, April 24, 2016

# It is required to design a circuit that counts the number of data transitions (i.e. 0→1and 1→0 data changes) through a stream of 128 bit data. The data is applied serially through an input *X* once the user presses a *Start* button, where the first bit is transmitted in the same cycle the *Start* button is asserted. Once the computation is finished the machine asserts a *Done* signal which remains asserted until the user presses the Start button again or resets the machine. Assume that the machine has Asynchronous *Reset* input. The ASMD chart for this machine is given below.



# Write a behavioral Verilog module to model the data path unit for the given ASMD chart for circuit.

module Quiz5DP(output reg [6:0] CNT2, output C1EZ, input Init, Dec1, Inc2, CLK);

reg [6:0] CNT1;

assign C1EZ= ~| CNT1;

always @(posedge CLK)

if (Init) begin

CNT1 <= 127;

CNT2 <= 0;

end

else begin

if (Dec1) CNT1 <= CNT1 - 1;

if (Inc2) CNT2 <= CNT2 + 1;

end

endmodule

# Write a behavioral Verilog module to model the control unit for the given ASMD chart for this circuit.

module Quiz5CU (output reg Init, Dec1, Inc2, Done, input X, Start, C1EZ, Reset, CLK);

parameter S0 = 2'b00, S1=2'b01, S2=2'b10, S3=2'b11;

reg [1:0] state, next\_state;

always @(posedge CLK, posedge Reset)

if (Reset) state <= S0;

else state <= next\_state;

always @(state, X, Start, C1EZ) begin

Init=0; Dec1=0; Inc2=0; Done=0;

case (state)

S0:

if (Start) begin

Init=1;

if (X) next\_state=S2;

else next\_state=S1;

end

else next\_state=S0;

S1:

if (C1EZ) begin

Done=1; next\_state=S3;

end

else begin

Dec1=1;

if (X) begin

Inc2 = 1;

next\_state=S2;

end

else next\_state=S1;

end

S2:

if (C1EZ) begin

Done=1; next\_state=S3;

end

else begin

Dec1=1;

if (!X) begin

Inc2 = 1;

next\_state=S1;

end

else next\_state=S2;

end

S3: begin Done=1;

if (Start) begin

Init=1;

if (X) next\_state=S2;

else next\_state=S1;

end

else next\_state=S3;

end

default: next\_state='bx;

endcase

end

endmodule

# Write a Verilog module to model the overall circuit by connecting the data path and control unit modules.

module Quiz5 (output [6:0] CNT, output Done, input X, Start, Reset, CLK);

Quiz5DP M1 (CNT, C1EZ, Init, Dec1, Inc2, CLK);

Quiz5CU M2 (Init, Dec1, Inc2, Done, X, Start, C1EZ, Reset, CLK);

endmodule