Name: Id#

COE 405, Term 152

 Design & Modeling of Digital Systems

Quiz# 4

Date: Sunday, April 14, 2016

#  It is required to design a circuit that receives two **4-bit** signed numbers in 2's complement representation **A=A3A2A1A0, B=B3B2B1B0** and produces a **6-bit output** **C= C5C4C3C2C1C0**. The circuit implements the following functions based on the values of the three selection inputs: S1, S1 and S0.

|  |  |
| --- | --- |
| S2 S1 S0 | Function  |
| 0 0 0  | C = A + B |
| 0 0 1 | C = A - B |
| 0 1 0 | C = A + 1 |
| 0 1 1 | C = A - 1 |
| 1 0 0  | C = 2\*A+B  |
| 1 0 1 | C = 2\*A-B |
| 1 1 0 | C = 2\*A+1 |
| 1 1 1 | C = 2\*A-1 |

# Show the block diagram design of your circuit using MSI components like Adder, Multiplexor, as needed. Use only one adder in your solution.

# Model your design in Verilog by modeling each component separately i.e. adder, MUX, etc. and then instantiate these components to model your circuit.

# Write a Behavioral Verilog model to model the given circuit.