Name: Id#

COE 405, Term 152

 Design & Modeling of Digital Systems

Quiz# 3

Date: Sunday, April 3, 2016

# **Q1**. Given below the design of an *n*-bit magnitude comparator. The circuit receives two *n*-bit unsigned numbers ***A*** *and* ***B*** and produces two outputs **GT** and **EQ** as given in the table to the right.

|  |  |
| --- | --- |
|  | **GT EQ** |
| IF A > B |  1 0 |
| IF A = B |  0 1 |
| IF A < B |  0 0 |



# The input operands are processed in a bitwise manner *starting with the most significant bit (MSB)*. The comparator circuit is constructed using *n identical copies* of the basic 1-bit *cell* shown to the right.

# The Figure below shows the *n*-bit comparator circuit implemented using *n* copies of the basic 1-bit cell.



# Boolean expressions of the outputs of ***cell i*** and its gate-level implementation are given below:

$GT\_{i}=GT\_{i+1}+A\_{i} \overbar{B}\_{i} EQ\_{i+1} $



Cell *i* Gate Level Implementation

*EQi =* (*Ai* 🞊 *Bi*). *EQi+1*

## Write a Verilog model **Comp1Bit** to model the 1-bit comparator circuit using *either* a structural model of basic logic gates *or* a behavioral model using the **assign** statement.

The declaration of the Comp1Bit module is as follows:

**module** Comp1Bit **(output** GT\_out, EQ\_out , **input** GT\_in , EQ\_in, Ai, Bi**);**

**endmodule**

## Complete the following Verilog model **Comp3Bit** that models a 3-bit comparator circuit.

**module** Comp3Bit **(output** Greater, Equal,  **input** [2:0] A , B**) ;**

**endmodule**

## Write a Verilog test bench to test the 3-bit comparator **Comp3Bit** by applying the following input patterns consecutively with a delay of 20ps:

## {A=100, B=011},

## {A=101, B=101},

## {A=011, B=111}.