Name: KEY Id#

COE 405, Term 152

Design & Modeling of Digital Systems

Quiz# 2

Date: Sunday, Feb. 28, 2016

# It is required to design a sequential circuit that has a single input X representing a signed 2's complement number and a single output Y. The circuit receives the number serially through the input X from the least significant bit (LSB) to the most significant bit (MSB), and computes the equation Y=X-3 and generates the output serially from the least significant bit to the most significant bit. The circuit has an additional asynchronous reset input R that resets the circuit into an initial state. The following are examples of input and output data:

Examples:

LSB

MSB

Output=3

Input=6

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Input | X | 0 | 1 | 1 | 0 | 0 |
| Output | Y | 1 | 1 | 0 | 0 | 0 |

MSB

LSB

Output=9

Input=12

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Input | X | 0 | 0 | 1 | 1 | 0 |
| Output | Y | 1 | 0 | 0 | 1 | 0 |

## Draw a state diagram or show the state table of the circuit with minimum number of states assuming a **Mealy** model. You are not required to implement the circuit.

|  |  |  |
| --- | --- | --- |
| **Present State** | **Next State, Y** | |
| **X=0** | **X=1** |
| S0 (B=3) | S1, 1 | S2, 0 |
| S1 (B=2) | S2, 0 | S2, 1 |
| S2 (B=1) | S2, 1 | S3, 0 |
| S3 (B=0) | S3, 0 | S3, 1 |

# Consider the given FSM that has 4states, one input X and one output Z, represented by the following state table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Present State** | **Next State, Z** | | | |
| **X=0** | | **X=1** | |
| S0 | S1, 0 | S2, 0 | |
| S1 | S0, 0 | S3, 0 | |
| S2 | S2, 0 | S3, 1 | |
| S3 | S3, 0 | S2, 1 | |

## Determine the equivalent states.

|  |  |  |  |
| --- | --- | --- | --- |
| S1 | (S2, S3) |  |  |
| S2 |  |  |  |
| S3 |  |  | √ |
|  | S0 | S1 | S2 |

## Thus, the equivalent states are (S0, S1) and (S2, S3).

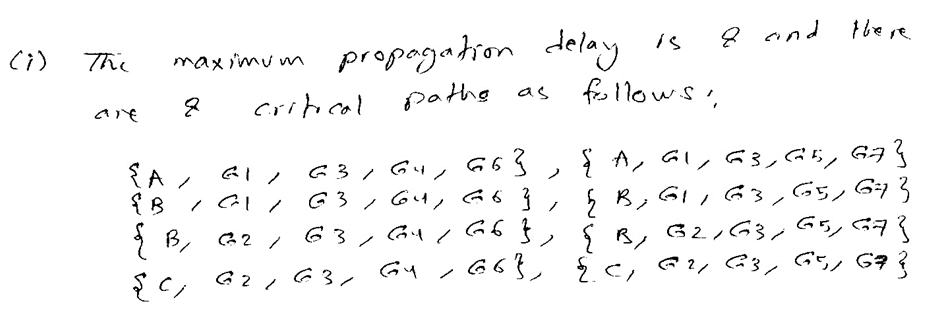
## Reduce the state table into the minimum number of states and show the reduced state table.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Present State** | **Next State, Z** | | | |
| **X=0** | | **X=1** | |
| S0 | S0, 0 | S2, 0 | |
| S2 | S2, 0 | S2, 1 | |

# Consider the sequential circuit given below having 5 inputs {A, B, C, D, E} and one output {Z}. Assume that the delay of a gate is related to the number of inputs i.e. the delay of a 2-input AND gate is 2 unit delays and the delay of a 2-input OR gate is 2 unit delays.

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## Determine the critical path of this circuit and the maximum propagation delay.



## Using only the **Retiming** transformation, reduce the critical path of this circuit with the minimum number of flip-flops possible. Determine the maximum propagation delay after retiming.

