KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 405 Design and Modeling of Digital Systems (3-0-3)
Syllabus - Term 181

Catalog Description

Digital design methodology. Review of combinational and sequential circuit design. Design of digital systems composed of data path and control units. Hardware description language-based modeling of digital systems. Synthesis and optimization of digital systems. Digital system design using field-programmable gate arrays (FPGAs).

Prerequisite: COE 202

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Office Hours ***UT 12:20-1:00 PM, MW 11:00-12:00 and by appointment***

Course Objectives

The objectives of this course are to introduce students to the design methodologies of digital systems with special emphasis on FPGA implementations.

Course Learning Outcomes

After completing the course, students should be able to:

i. Design optimized combinational and sequential circuits.
ii. Design and implement digital systems composed of data path and control units.
iii. Model and simulate digital systems using hardware description languages (Verilog HDL).
iv. Employ synthesis and optimization techniques at the gate and high levels.
v. Synthesize and implement digital systems using FPGAs.

Text book: M. D. Ciletti, "Advanced Digital Design with the Verilog HDL," (Prentice Hall), 2/e 2010.

References:

1. "Verilog Styles for Synthesis of Digital Systems", David R. Smith and Paul D. Franzon, Prentice Hall, ISBN 0-201-61860-5
2. Online Verilog resources:
    i. http://www.doulos.com/knowhow/verilog_designers_guide/
    ii. http://www.sutherland-hdl.com/online_verilog_ref_guide/vlog_ref_top.html

Grading Policy

Discussions	3%	
Assignments	15%	
Quizzes	12%	
Midterm	25%	**(Sat. Oct. 27, 10:00 AM)**
Project	20%	
Final	25%	

- Attendance will be taken regularly. The tenth unexcused absence results in a DN grade
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted (upto 3 days) but you will be penalized 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 15%.
- No makeup will be made for missing Quizzes or Exams.

Course Outline:

List of Topics	Contact Hours
Digital Design Methodology: Digital system design cycle, design space and evaluation space, digital system complexity, dealing with design complexity, design hierarchy, abstractions, design domains & levels of abstraction, design methods, design vs. synthesis, synthesis process, design automation & CAD tools.	3
Combinational Circuit Design: Review of simplification procedure, don't care conditions, design of combinational circuits.	2
Sequential Circuit Design: Review of sequential circuit models: Mealy vs Moore, state assignment, state minimization, sequential circuit timing, timing constraints, flip-flop set up time, Clock to Q delay, flip-flop hold time, clock skew, peak to peak jitter, hold time violation, metastability, synchronization.	4
Design of Digital Systems: Data path & control unit partitioning, data path design, algorithmic state machine (ASM) chart, control unit design, examples of digital system design, design of sequential multiplication and division circuits.	9

HDL Modeling of Digital Systems: Gate-level modeling, Verilog primitives, Verilog syntax, Verilog data types, module instantiation, organization of a Testbench, delay modeling, modeling iterative circuits using generate construct, behavioral modeling, data types for behavioral modeling, Verilog operators, always block, procedural assignment, wire vs. reg, algorithm-based models, if statement, case statement, behavioral models of combinational and sequential blocks, FSM and ASM chart behavioral modeling, repetitive algorithms: for loop, repeat loop, while loop, disable, forever, tasks and functions, register file, memory unit, file I/O system functions and tasks, Behavioral and timing simulations.	9
Synthesis and Optimization of Digital Systems: Multilevel logic transformations, synthesis & testability, critical path, delay minimization, behavioral or high-level synthesis: CDFG, scheduling, allocation, HDL modeling styles for synthesis, avoiding inferred latches, exploiting don't care conditions, synthesis of three-state devices and bus interfaces, synthesis of loops. Pipelining and register re-timing, data streaming, and moving data across multiple clock domains.	11
Digital System Design using FPGAs: History of computational fabrics, ASIC vs. FPGA, reconfigurable logic, anti-fuse-based approach, RAM based field programmable logic, FPGAs architecture, LUT-based RAMs, Block RAMs, synthesis flow in FPGAs, design and implementation using FPGAs. Clocking, using HW macros, and I/O standards. Simulations.	7
Total	45